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A DSP Implementation of Embedded Zerotree Wavelet (EZW) Image CODEC in Image Compression System

Shamika M. Jog [1], Shashikant. D. Lokhande [2]
[1] Cummins College of Engineering, Pune, India
Email: shamika_jog@yahoo.co.in
[2] Sinhgad College of Engineering, Pune, India
Email: {sdlokhande.scoe}@ sinhgadedu.com

***Abstract*— Digital image compression is a very popular topic in the field of multimedia processing. The major focus of work is to develop different compression schemes/algorithms to provide good visual quality fewer bit to represent an image in digital format.**

This paper work describes software and hardware implementation of Embedded Zerotree Wavelet (EZW) image Coder-Decoder (CODEC).The EZW image CODEC is used to compress and decompress gray scale image in image compression system. Here, EZW CODEC is implemented by Texas Instruments Digital Signal Processor (DSP) TMS320C6713 board. The EZW CODEC algorithms has been transferred into C and assembly code in Code Composer Studio (CCS) in order to program the C6713 DSP processor. The statistical analysis is also carried out with profile statistic available in CCS environment.

With the development tools provided for the C6713 DSP platform, it created easy-to-use environment that optimizes the devices' performance and minimizes technical barriers to software and hardware design

***Index Terms*—Image Compression, Redundancy, EZW, CODEC.**

I. Introduction

With the growth of technology and the entrance into the Digital Age, the world has found itself a vast amount of information. Dealing with such enormous amount of information can often present difficulties. Digital information must be stored, retrieved, analyzed and processed in an efficient manner, in order for it to be put to practical use.

A. Need for Compression

Today is an era of internet, images, motion pictures etc. Transmission and usage of image can not be avoided. Image compression is a technique which makes storage and transmission of images more practical. the basic requirement of maintaining image quality is easily translated into two basic quantitative parameters:

1) Rate of digital image data transfer or data rate (Megabit per second or Mb/s)
2) Total amount of digital storage required or data.

With image compression both data rate and data capacity are reduced to great extent. So less space, less time and less bandwidth are required for storage and transmission of digital images.

B. Fundamentals in Compression

The fundamental components of compression are redundancy and irrelevancy reduction. Redundancy means duplication and Irrelevancy means the parts of signal that will not be noticed by the signal receiver, which is the Human Visual System (HVS). Image compression focuses on reducing the number of bits needed to represent an image by removing the spatial and spectral redundancies.

C. Basic types of image compression

Basic types of image compression are lossless and lossy. Lossless compression works by compressing the overall image without removing any of the image's detail. Lossy compression works by removing image detail, but not in such a way that it is apparent to the viewer [1, 2].

The organization of the paper is as follows: Section II provides the information about literature survey. Section III focuses on Embedded Zerotree Wavelet (EZW) algorithm for image compression. Section IV describes the Digital Signal Processing (DSP) architecture selection. Section V provides description of the DSP implementation of EZW image CODEC. Section VI shows results and finally section VII concludes the paper.

II. Literature survey

Over the past few years, a variety of novel and sophisticated wavelet-based image coding schemes have been developed. These include Embedded Zerotree Wavelet (EZW) algorithm, Set Partitioning in Hierarchical Trees (SPIHT) algorithm, Embedded Block Coding with Optimized Truncation (EBCOT), Lossless image compression using Integer Wavelet Transform (IWT), Image coding using adaptive wavelets. This list is by no means exhaustive and many more such innovative techniques are being developed as this article is written. I will briefly discuss a few points of these interesting algorithms here.

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A. Embedded Zerotree Wavelet (EZW) Algorithm

When searching through wavelet literature for image compression schemes, it is almost impossible not to note Shapiro's Embedded Zerotree Wavelet encoder or EZW encoder. The EZW encoder was originally designed to operate on images (2D-signals) but it can also be used on other dimensional signals.The EZW encoder is based on progressive encoding to compress an image into a bit stream with increasing accuracy.

B. Set Partitioning In Hierarchical Trees (SPIHT) Algorithm

Said and Pearlman, offered an alternative explanation of the principles of operation of the EZW algorithm to better understand the reasons for its excellent performance. According to them, partial ordering by magnitude of the transformed coefficients with a set partitioning sorting algorithm, ordered bit plane transmission of refinement bits.

C. Scalable Image Compression with EBCOT

This algorithm is based on independent Embedded Block Coding with Optimized Truncation (EBCOT) of the embedded bit-streams which identifies some of the major contributions of the algorithm. The EBCOT algorithm is related in various degrees to much earlier work on scalable image compression.

D. Image Coding using Adaptive Wavelets

In wavelet-based image coding, the wavelet filter can be chosen adaptively depending on the statistical nature of image being coded [1, 2, 3].

III. Embedded Zerotree Wavelet (EZW) Algorithm

An EZW encoder is an encoder specially designed to use with wavelet transforms. Here, EZW algorithm is selected due to following features:-

1. Discrete Wavelet Transform which provides compact multi-resolution presentation of image.
2. Zerotree coding which provides compact multi-resolution presentation of significant maps, which are binary maps indicating positions of significant coefficients.
3. Successive Approximations which provides multi-precision presentation of significant coefficients.
4. Larger coefficients are more important than smaller coeffients regardless their scales.
5. The algorithm runs sequentially and stops whenever target bit rate or target distortion rate is met [3, 4].

IV. DSP Architecture Selection

There are two types of programmable DSP: fixed point DSP and floating point DSP. Fixed point DSP is cheaper, faster and is suitable for large volume production. The Texas Instruments TI TMS320C613 is the latest and highest performance floating point DSP processor. These processors are 10 times faster than any other processor on the market at the present time, which are 2400 million instructions per second (MIPS) at 300 MHz**.** The interior configuration of the DSP uses Harvard configuration. The program memory and data memory are separated in this kind of configurations. It has specific hardware multipliers and the pipelining technology is widely used in DSP. In addition, over recent years, as the performance-price ratio of the DSP chips become higher and higher, the DSP is introduced to more widely applications [5, 7]

V. DSP Implementation of EZW Image CODEC

The paper describes the implementation of the EZW image CODEC (Encoder and Decoder) by using the Texas Instruments DSP (Digital Signal Processor) TMS320C6713 board. The EZW CODEC software is written in C and assembly code, which allows the code to be changed, updated and modified easily by using Code Composer Studio.

"Fig. 2'' shows typical EZW image CODEC system. It comprises of three main stages: transformation (wavelet decomposition), quantization and coding by rounding to the nearest integer.

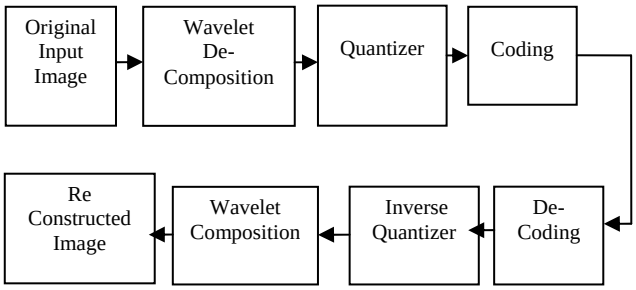

Figure 2. Block diagram of EZW image CODEC.

A. Transformation

The principle of wavelet image coding is based on the decomposition of an image into a number of frequency bands referred to as sub-bands.

B. Quantization

Each sub bands are quantized using uniform scalar quantizer, which is used to control the total bit rate

C. Coding

The quantizer stage will be followed, by the scanning process, zero run length coding and Huffman coding. To reconstruct the image, the decoder basically performs the three main inverse operations in reverse order [3, 6].

VI. Results

EZW algorithm is applied on 8x8 size image matrix as shown in "Fig. 3,". With EZW algorithm, embedded bit stream is generated at the output of EZW encoder. This bit stream is then applied as a input to EZW decoder and reconstructed matrix is same as that of original matrix.

63	-34	49	10	7	13	-12	7
-31	23	14	-13	3	4	6	-1
15	14	3	-12	5	-7	3	9
- 9	-7	-14	8	4	-2	3	2
-5	9	-1	47	4	6	-2	2
3	0	-3	2	3	-2	0	4
2	-3	6	-4	3	6	3	6
5	11	5	6	0	3	-4	4

pnztpttttztttttttptt1010ztnpttttttttt100110zzzzzppnpppnttnnp
tpttnttttttttptttptttttttttptttttttttttt1001110111101101100 0zz
zzzzztztznzzzzpttptpptpnptnttttptpnpppptttptptttpnp1101
1111011001000001110110100010010101100zzzzztzzzzz
tpzzzttptttnptpptptttnppnttttpnnpttpttpptttt101111001101
0001011111010110110010000000011011011001100011
1zzzttztttztttttnnttt

Figure 3 8x8 size image matrix and encoded bit stream

A. Comment on Encoder and Decoder Outputs

The output of EZW encoder is an EZW bit stream. the **".ezw"** file generated from the encoder which consists of a text header followed by the output from the dominant and subordinate phase encoding as a stream of text symbols. I've used following symbols in the encoded format. '**p**' is a positive coefficient greater than the current threshold.,'**n**' is a negative coefficient greater than the current threshold.'**z**' is a an isolated zero, or a coefficient that is below the current threshold but is not a zerotree root.'**t**' is a zero tree root. This coefficient and all of its descendants are below the current threshold.'1'is '1' output from the subordinate phase and '0'is '0' output from the subordinate phase.

For EZW decoder, input is EZW bit-stream and its output is 8x8 size image matrix which is same as original matrix. Decoding the EZW data stream also uses dominant and subordinate passes. Following tables gives analysis of EZW algorithm in Code Composer Studio (CCS) environment.

Table 1 EZW Encoder

Symbol Name	cycle.Total: Incl. Total	cycle.Total: Excl. Total
EZW_code	34869	247
append_to_list	1054	240
code	7107	1319
destroy_fifo	35	35
destroy_list	1025	88
dominant_pass	18602	1270

Table 2 EZW Decoder

Symbol Name	cycle.Total: Incl. Total	cycle.Total: Excl. Total
EZW_decode	37916	263
append_to_list	1373	429
destroy_fifo	41	41
destroy_list	981	124
dominant_pass	28762	1618

Here, two separate modules have been created **(encoder.pjt and test.pjt)** in Code composer Studio (CCS). Statistical analysis is done by using the profile statistic of Code Composer Studio. Here, EZW encoder and decoder outputs are studied with and without compiler optimization levels. With level 02 optimization technique, number of total cycles are reduced as compared with no optimization applied. From the DSP perspective, several options are used to improve the execution speed.

VII. Conclusion

The EZW CODEC is successfully implemented on floating point DSP TMS320C6713. The program is written in Visual C++ and assembly language to achieve fast program execution. The capability of the C6713 to change the code easily and update applications have reducing the development time and cost. Besides, with the development tools provided for the C6xx DSP platform, it created easy-to-use environment that optimizes the devices' performance and minimizes technical barriers to software and hardware design. The number of cycles required to execute functions can still be reduced with better optimization techniques.

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