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Options for Ground Fault Clearance in HVDC Offshore Networks

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Abstract— **The unavailability of adequate HVDC circuit breakers is often named as one of the key inhibitors for building HVDC multi-terminal networks. Instead of only discussing what needs to be done with respect to improving CB technology, we discuss what other options in principle exist. None of the options is optimum in itself, thus the discussion must be mainly driven by reviewing the pros and cons from a fault current clearing point of view and also from a network planning and operation point of view. The manuscript aims at triggering and stimulating the discussion on fault clearance options other than only CBs.**

I. INTRODUCTION

Offshore wind farms are widely recognized as a key component of Europe's roadmap towards a low carbon electricity supply. The installed capacity of fully commissioned offshore wind turbines in Europe is in excess of 3200 MW, with another 3850 MW currently under construction and significantly more installations planned [1]. So far, the power transmissionfrom offshore wind farms has been exclusively based on point-to-point connections (either using HVAC or HVDC submarine cables). However, academics, industry consortiums, and environmental NGOs have all expressed significant interest in the idea of creating an interconnected offshore power network [2], [3], [4], [5], [6]. Expected benefits include increased system redundancy, higher flexibility for power trading, and reduced investment and operational costs.

As HVAC cables are not technically viable for long transmission distances, and traditional current source converter (CSC) based HVDC systems are not well suited for multi-terminal operation [7], the key enabling technology for such networks is widely recognized to be voltage source converter (VSC) HVDC. Their advantage is the ability to support the voltage at weak AC grid locations through independent reactive power control and the black-start capability.

The various plans for offshore DC grids envision the creation of so-called offshore supernodes, which provide the function of power collection and routing [3]. These nodes would couple the wind farm collection grids (which could be either AC or DC [8]) to other onshore or offshore HVDC substations.

Grid protection is currently one of the main obstacles for multi-terminal VSC networks. While AC side circuit breakers (CBs) can adequately protect point-to-point HVDC connections, the same protection approach would not be acceptable for HVDC grids, as it requires the de-energization of the entire system [9], [10]. DC CBs are needed to selectively isolate a faulty cable by quickly and reliably breaking DC fault currents. As will be discussed in this paper, the promising DC CB technologies still have significant drawbacks in terms of on-state losses or speed. The application of the well-known AC fault clearance concept to DC networks, in which CBs are placed at the ends of each line, is questionable. Other concepts to address fault clearance have to be chosen as long as no fully satisfying DC CB concept is developed. Options for fault clearance are the choice of converter technology and filter size, the choice of the grounding scheme, the layout of the network, or the support of the CBs by fault current limiters (FCLs).

The goal of this manuscript is not to analyze all of these options in detail, but to start the thinking off the beaten track and to contribute to promote the discussion for options other than the classical concept of relying only on CBs.

While submarine cable faults are less frequent than overhead line faults, but typically permanent, it is still a condition that a future DC network needs to be prepared for. The emphasis in this paper is on pole-to-ground faults, since they are regarded as significantly more frequent compared to pole-to-pole faults [12], although the latter fault would lead to more severe conditions [13].

The paper is structured as follows: In section II, the prospective transient short-circuit currents are calculated for a typical small offshore DC network. An overview of DC-CB technologies and an estimation of their performance limits is given in Section III. As can be seen, no CB technology is able to cope with the short-circuit currents that occur even in this small example network. In Section IV, we thus describe other options for fault clearance that either support a breaker by reducing the amplitude or the rate of rise of the fault current or even those that do not need DC-CBs. None of these options is optimum, but a trade-off with respect to losses or system performance has to be made. These aspects are discussed in Section V, which closes this paper.

II. SHORT CIRCUIT DEVELOPMENT IN OFFSHORE NETWORKS

A. Test System

Short circuit current developments and fault current reduction options will be discussed using the example of a four-terminal VSC-HVDC grid (cf. also Figure 1). The system represents a radial connection of an offshore wind farm node to three onshore nodes and is loosely based on a possible connection grid of the Kriegers Flak wind farm in the Baltic Sea [14].

The converters are modeled as a ±320 kV bipolar two-level VSC topology with concentrated midpoint-grounded DC filter capacitors at each terminal. However, the analysis of pole-to-ground faults presented in this paper would be equally valid for a system based on asymmetrical monopoles or a mixture of the two. The system is modeled in PSCAD-EMTDC and makes use of a detailed frequency dependent, distributed-parameter cable model. The general design of the cable cross-section is derived from a real 150 kV XLPE VSC-HVDC submarine cable [15], [16]. The cross-section was scaled up to a 320 kV cable respecting the diameter of the cupper conductor [17], while keeping the electric field stress (cold condition) similar. The material properties are based on values given in [18]. TABLE I. summarizes the cable cross-section dimensions and material properties.

TABLE I. PROPERTIES OF ASSUMED 320 KV XLPE CABLE

Layer	Material	Outer radius (mm)	Resistivity (Ωm)	Rel. permittivity	Rel. permeability
Core	Copper	21.4	$1.72 \cdot 10^{-8}$	1	1
Insulation	XLPE	45.9[a]	-	2.3	1
Sheath	Lead	49.4	$2.2 \cdot 10^{-7}$	1	1
Insulation	XLPE	52.4	-	2.3	1
Armor	Steel	57.9	$1.8 \cdot 10^{-7}$	1	10
Insulation	PP	61.0	-	2.1	1

a. Including inner and outer semi-conductor layer of 1.2 and 1.3 mm thickness, respectively.

The example DC network is connected to four AC nodes, one offshore wind farm (WF) and three countries connected radially to WF. Node "N" is located 55 km north, "W" 75 km west, and "S" 130 km south of the wind farm. All AC nodes are assumed identical for simplicity and their short circuit behavior is modeled as that of a voltage source behind an inductance. In reality, their behavior might vary considerably. In particular, the representation of the short circuit current contribution of wind farms deserves further and more detailed attention. The connection to the converters is made via transformers with grounded Y-windings on the grid side and Δ-connection on the converter side. The chosen fault resistance of $R_f = 7\ \Omega$ is based on the impulse behavior of concentrated grounds at high currents [19] and corresponds to the resistance at the peak current of a sparking connection in wet loamy sand. The parameters of the test system in its base case configuration are summarized in TABLE II.

TABLE II. TEST SYSTEM PARAMETER (BASE CASE)

Parameter	*Value*
Rated Converter Power (Bipole)	900 MW
DC Voltage	±320 kV
DC Filter Capacitances (pole to ground)	100 µF
AC Voltage Grid Side (L-L, RMS)	380 kV
AC Voltage Converter Side (L-L, RMS)	395 kV
Short Circuit Power of AC Nodes	4500 MVA
X/R of AC networks	∞
Fault Resistance (R_f)	7 Ω
Transformer Leakage Reactance	0.1 pu
Converter Phase Reactor	0.1 pu

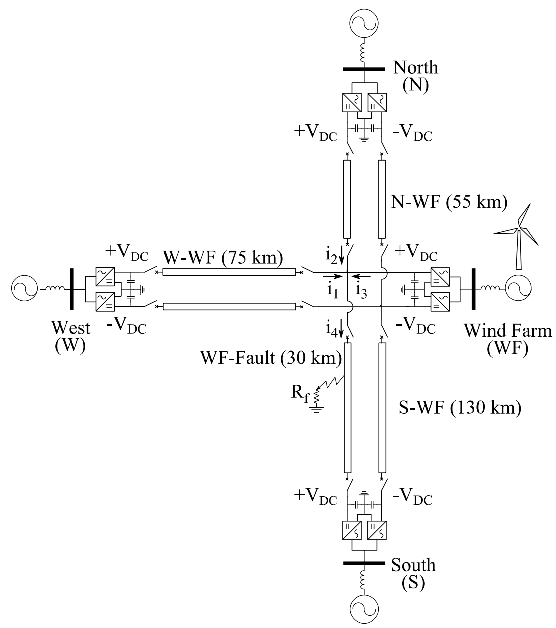


Figure 1. Four-terminal VSC-HVDC test system.

B. Short Circuit Current Development in Base Case

In this section, the short-circuit current resulting from a pole-to-ground fault on the positive pole on the line connecting WF and S is modeled to show the principle behavior of the transient fault current development. In this scenario, the current i_4 in the positive pole from WF to S corresponds to the highest fault current that a potential DC circuit breaker would be subjected to. This current is the sum of the fault current contributions from all lines and the converters at WF, N, and W, indicated as i_1, i_2 and i_3, respectively. The fault occurs at t = 0 ms. All four currents are shown in Figure 2

The upper part of Fig. 2 shows that in the absence of any clearance action, the development of the fault currents can be divided into a transient period (approximately the first 50 ms) and a steady-state period. The transient period is characterized by the discharge of passive circuit elements (primarily filter and cable capacitances), whereas the steady-state currents are directly linked to fault currents fed into the DC system from the AC side. The latter phenomenon is a characteristic of a pole-to-ground fault in a bipolar system, in which the fault creates a ground loop through the neutral of the filter capacitors. As soon as the DC voltage in the positive pole drops below the instantaneous converter AC bus voltage of one of the phases, the converter, in which the IGBTs are assumed to be instantaneously blocked for self-protection, becomes an uncontrolled diode rectifier [20], allows the AC system to feed the DC fault. Even though the distance of the three feeding terminals varies between 0 and 75 km, the mean steady-state values of i_1, i_2 and i_3 deviate approximately 2% from each other, reflecting the low impedance of the DC cables.

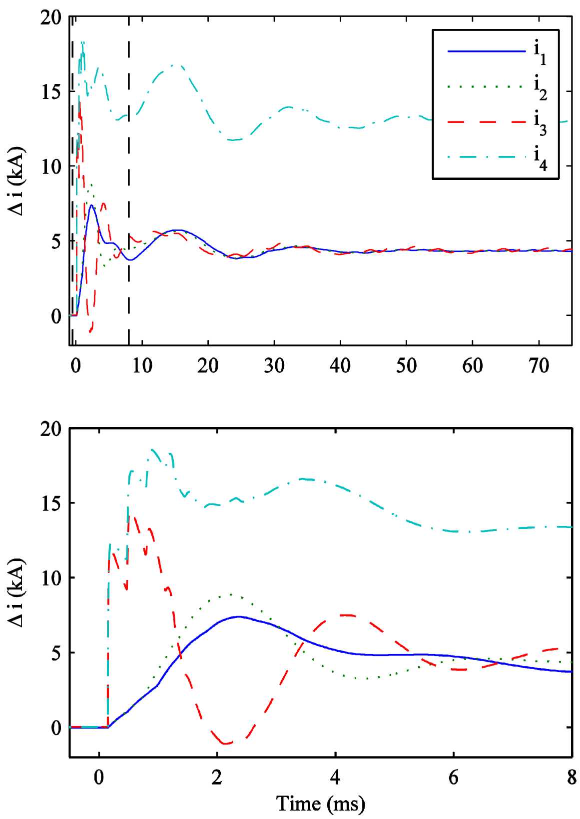


Figure 2. Short circuit currents in for pole-to-ground fault in four-terminal test system using base case parameters.

The lower part of Figure 2 shows a magnified view of the same quantities for the first 8 ms. The short time delay between the fault occurrence and the time at which the currents start rising corresponds to the travel time of the negative voltage wave from the fault location to WP. In the next 1 ms, i_4 is characterized by a series of peaks originating from discharges of the filter capacitances at WP caused by successive arrivals of reflections of the initial voltage wave. The transient contributions from the W and N feeder, i_1 and i_2, are characterized by a much slower rate of rise, representing a gradual discharge of the distributed cable capacitances.

III. Technologies for HVDC Circuit Breakers

The extremely high short-circuit current gradients in the modeled test system clearly identified the time of current interruption (the time until fault current limitation takes effect) as the most relevant parameter for the choice of breaker technology. TABLE III. compares promising technologies with respect to their total interruption time, on state losses, and state of development.

A. *Full Solid State CB*

Topologies for full solid state breakers are typically are based on a certain number of GCTs, GTOs or IGBTs connected in series [21], [22]. The reaction times are extremely fast, which makes them ideal DC circuit breakers. Drawbacks are mainly the substantial on state losses (especially for IGBTs) and the high component costs. This inhibits full solid state breakers to be utilized in large numbers. So far, only applications in MV DC- and AC-networks have been proposed [21], [23]. HVDC multi-terminal network applications, where speed is a crucial factor should be considered instead. Advances in semiconductor device technology such as higher blocking voltages, lower forward losses or even new materials may be a key promoter for the full solid state CBs.

B. *Hybrid Solid State CB with Mechanical Disconnector*

Hybrid solid state CBs comprise a current interruption and a current conduction path. One proposed solution consists of a fast, but small solid state switch in series with a fast metal contact disconnector in the main path [25]. The actual breaker is located in a parallel path and consists of a number of series connected solid state switches. The small IGBT in the main path needs only to create a sufficiently high voltage for the commutation of the current to the parallel full IGBT breaker. The main path requires, therefore, fewer modules in series and, thus, features a smaller forward voltage and lower on state losses compared to the full IGBT breaker. The disadvantage of this arrangement is the increased interruption time due to the required opening time of the mechanical disconnector. The concept is very attractive, but the costs of the IGBT modules remain the same.

C. *Hybrid Mechanical and Solid State CB*

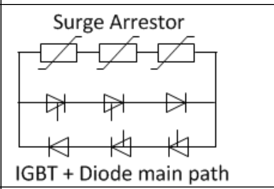
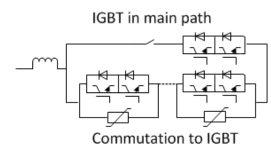
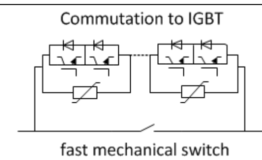
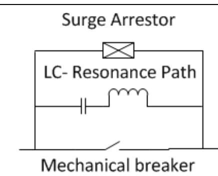
Hybrid mechanical solid state breakers combine the low forward losses of a pure (fast) mechanical breaker and the fast performance of a solid state breaker in the parallel path [21]. They are faster than common mechanical breakers, as the arc chamber must only create sufficient voltage for commutation, but no artificial current zero crossing. They are beneficial over hybrid solid state breakers, only if the contact separation speed and, thus, the buildup of arc voltage for commutation can be significantly increased or if measures in the grid allow interruption times >20ms. So far, ultrafast switches have been designed and tested only for MV levels [26], [27].

D. Mechanical Passive or Active Resonance CB

Mechanical passive or active resonance breakers have been developed for CSC HVDC systems and are based on AC gas circuit breakers. An additional LC-commutation circuit is placed in parallel to the CB. This enables a current oscillation between the two parallel paths and may create an artificial current zero crossing in the main path at which the CB can interrupt [29], [30]. The oscillation can be achieved by an active current injection from a pre-charged capacitor or excited passively by the arc. Yet, no technical solution has been found to overcome the maximal interruptible current for passive resonance breakers, which is a consequence of the positive UI-arc characteristics at high currents. Active resonance breakers create the current zero with pre-charged capacitors and are, therefore, not bound to this limit. However, considerable capacitor size (especially at high voltage levels) results and no open-close-open switching operations are possible.

The low costs and low on state losses of mechanical breakers would allow them to be installed in large numbers. Due to their long interruption times, they are only effective in combination with fault limiting devices or in combination with faster breakers at critical locations. They should certainly be considered as DC load break switches.

TABLE III. BREAKER TECHNOLOGIES

	a) Full Solid State Breakers	**b) Hybrid Solid State CB with mech. disconnector**	**c) Hybrid Mechanical and Solid State CB**	**d) Mechanical passive or active resonance CB**
Typical breaker structure				
Expected total interruption time	<1ms	<2ms	<5-30ms	<60ms
Required times for • commutation and • energy absorption	<0.1ms for commutation ~1ms energy absorption	<0.2ms for commutation <1ms for disconnector opening ~1ms energy absorption	~20ms for contact separation (conventional AC breakers) ~1-5ms for magnetically driven UFS (Ultra-Fast Switch) with opening speed >20m/s)	~20ms for contact separation current zero creation ~30ms (passive resonance) ~2ms (active resonance)
Current state of development	- not yet built for HVDC - development of VSC and CSC boosts technology as components are alike	- working principle proved - type test and interruption test with downscaled breaker passed	- not yet available - slow AC breakers available - UFS not yet available	- applied in CSC HVDC - also used as MRTB (Metal Return Transfer Breaker)
Maximal rated voltage Un	≤800kV (same as voltage level)	120kV verified by test (up to 320kV achievable)	AC circuit breakers >500kV Ultra-Fast-Switches <12kV	≤550kV available
Max DC Breaking current In	<5kA expected	9kA experimentally proven (up to 16kA expected)	~6-12kA (estimated)	- up to 4kA proven in operation (up to 8kA possible with active resonance) - possible to survive transient overcurrents
Expected power loss in comparison to a VSC converter station	<30% (large forward voltage due to serial connection of solid state devices)	<1% (only few IGBTs in series in the main path)	<0.001% (metal contacts)	<0.001% (metal contacts)
Further development steps	- development in solid state device technology to reduce on-state forward voltage and number of modules in series	- field experience with prototype in a test grid - reduction of IGBT costs	- development of ultra-fast-mechanical drives to reduce commutation time	- optimization of DC arc chamber for passive resonance to achieve higher current rating and to minimize time for current zero creation

IV. FAULT CLEARING OPTIONS IN HVDC OFFSHORE NETWORKS

The two previous sections demonstrated that high levels and rates of rise of fault currents can occur in DC grids and that they exceed the capabilities of the interruption technology that is available today. Ways of easing the requirements of CBs through measures that affect the rate of rise, peak overshoot, or steady state of the fault current should therefore be investigated.

The presented options can be grouped into two general categories: options that do not affect the mean steady state fault current (Options 1) and 2)), and those that do (the remaining five options).

1) Reducing Size of Dischargable DC Filter Capacitors: Concentrated DC filter capacitors contribute significantly to the initial transient current peaks. Due to their proximity to potential feeder CBs, they lead to very high rates of rise. DC grid designs that rely on smaller capacitors or employ converter topologies, in which the DC capacitors cannot be discharged into a DC fault, such as in the Modular Multilevel Converter (MMC) concept [32], can thus be advantageous. Curve B in Figure 3 shows i_4 for a case with filter capacitances of 10 µF compared to 100 µF in the base case (curve A). It can be seen that the magnitude of the initial current peak is reduced. However, during subsequent transients ($5 < t < 20$ ms), there are periods, during which the current is actually higher than in the base case. A faster voltage drop and, thus, an earlier initiation of the AC feeding phase might contribute to these transients.

2) Adding Concentrated DC-Feeder Inductors: The initial rate of rise can be significantly lowered through additional inductors. Curve C shows i_4 for a scenario, in which a 200 mH inductor is placed at the end of each feeder. The occurrence of the peak current is shifted by around 35 ms.

While this can ease the di/dt requirements and allow a fast breaker to interrupt at a lower current, the addition of inductors needs to be carefully balanced with the control performance of the system, which relies on current changes for power flow control.

3) Reducing Short Circuit Power of AC Nodes: Reducing the short circuit power of the AC nodes reduces the steady state fault currents, but does not influence the initial transients. This is represented by curve D, for which a short circuit power of 2250 MVA (instead of 4500 MVA) was assumed.

The network protection scheme has to take into accont the short circuit capability of the individual AC nodes, particularly in schemes, which allow the implementation of slow DC CBs (i.e. with interruption times of > 20 ms) The current that needs to be interrupted in this case would directly depend on the combined strength of the AC nodes that are feeding the fault through that location. Short circuit limiting options include additional AC side reactors, thyristor controlled series inductors, or AC side superconducting fault current limitters (SCFCL) [34].

4) Using DC side SCFCLs: The idea of using resistive DC side SCFCLs for DC grid protection has been proposed by [35]. SCFCLs are characterized by a very rapid transition from zero resistance to their nominal conducting resistance once a critical current density is reached. SCFCLs would most likely be based on High Temperature Superconductors (HTS), which can be cooled with liquid nitrogen.

A very simple FCL model was implemented in series to the circuit breaker under consideration with a critical current of 2.1 kA (1.5 pu) and a nominal conducting resistance of 100 Ω. Curve E in Figure 3 demonstrates that the SCFCL limits the magnitude of the initial peak to less than half of the peak in the base case and reduces the fault current to below 3 kA within the first few ms and to around 3.8 kA in the steady-state period.

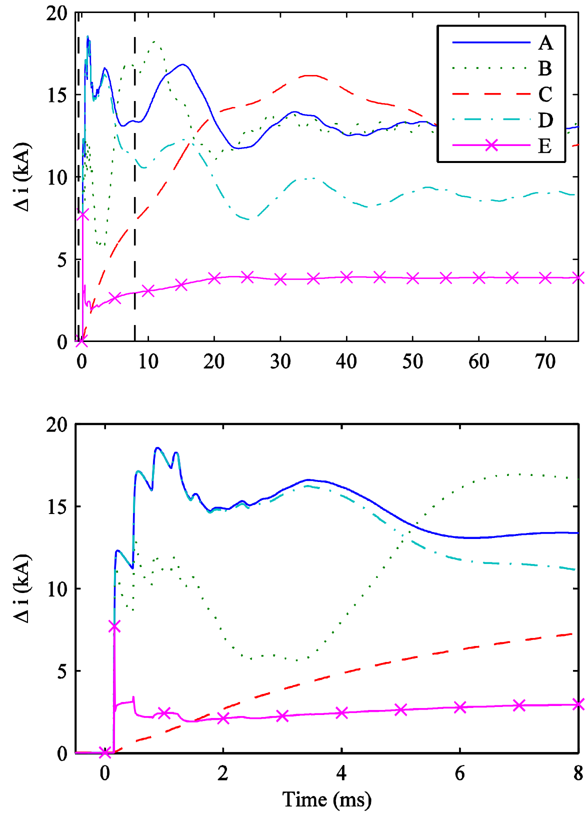


Figure 3. Fault current, i_4, for different current reduction options described in the text.

The simplified model of the SCFCL used in the simulation yields only indicative resultsand a more detailed model is necessary to fully assess the potential of SCFCLs in DC grids. The dissipation of heat is the main limiting factor. In this particular example, the energy converted into heat due to I^2R-losses amounts to around 7 MJ in the first 10 ms.

5) Full Bridge Converter Topologies: Full bridge converters [32], [33] inhibit the fault current contribution of the AC side through blocking of the reverse biased IGBTs. The inital fault current in a network employing full bridge converters exhibits a similar development as compared to the base case, whereas the current decreases to zero within approximately 15 ms (not shown in Figure 3) in a full bridge scheme.

Full bridge converters might be able to eliminate the need for separate CBs, if they are combined with fast acting disconnectors to isolate the faulty feeders [4]. The significant drawbacks, however, are the increased steady state losses, which are estimated to be 30 to 50% higher than in half-bridge converter designs [4], and the higher costs due the increased number of IGBTs. In addition, the network would need to be de-energized completely, though only for a short time, to clear a fault [22].

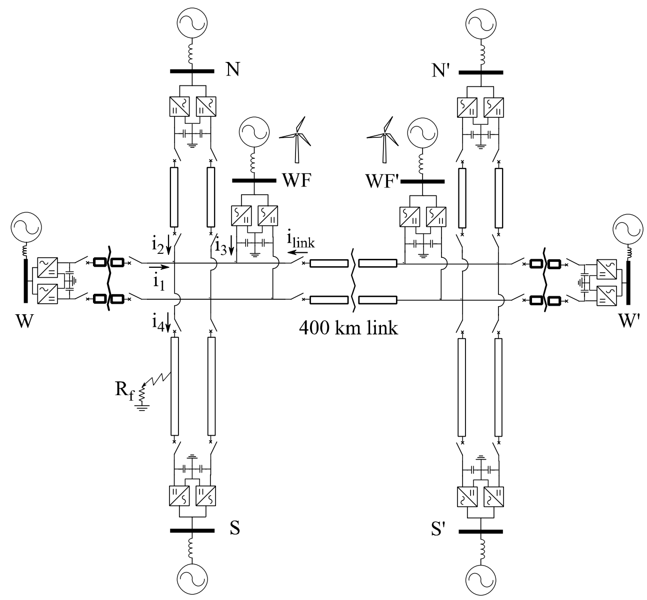


Figure 4. Modified system for investigation of selective placing of CBs.

6) Isolated DC Circuits [4]: A symmetrical monopolar VSC HVDC configuration isolates the DC side from the AC side in case of a pole-to-ground fault. The resulting short circuit current behavior is similar to that described in 5), where only passive elements contribute to the fault current (this option is also not shown in Figure 3).

Drawbacks of the symmetrical monopolar scheme are the overvoltages on the healthy pole due to the charging of the corresponding filter capacitor and the reduced redudancy compared to bipolar systems. In order to achieve redundancy, two parallel symmetrical monopolar systems are required (with a total of 4 (high voltage) cables).

7) Selective Placing of High Performance CBs at Strategic Grid Locations: The last fault current reduction option that is presented in this paper refers to the possibility of employing fast acting CBs or FCLs (or a combination of the two) on grid connections that have a large impact on potential fault currents in other parts of the network. The system that was considered so far (Figure 1) is not suitable for investigations of this type, since all three cable connections can be considered to be of equal importance in terms of their fault current contribution. Therefore, a modified system was created, in which the original system was copied and mirrored (Figure 4). Both individual networks are connected with an additional 400 km submarine cable link between the original WF node and the mirrored WF node (denoted as WF').

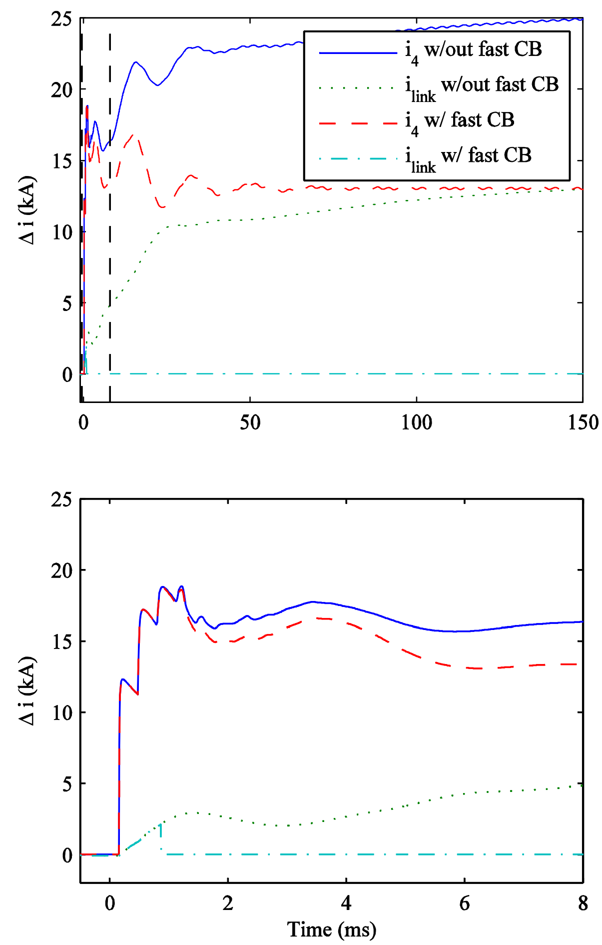


Figure 5. Fault current contribution from mirrored subsystem, i_{link}, to the fault current i_4 with and without a fast CB at location of i_{link}.

The fault type and location is identical to the previous investigations. The current i_4 through the breaker on the faulted line is now the algebraic sum of i_1, i_2, i_3 and i_{link}. Figure 5 illustrates that in absence of a breaking device in the interlink, the fault current contribution from the mirrored system is significant. While the rise i_{link} is relatively gradual, its contribution to current i_4 after 25 ms is nearly 50%.

In order to demonstrate the principle of this approach, a hypothetical fast CB is placed at the location of i_{link}. It is capable of interrupting the fault current as soon as it reaches 2.1 kA (1.5 p.u.) (cf. Figure 5). The effect of such a hypothetical device in the interlink is twofold: on the one hand, the subsystem without fault can continue to operate, though with a distorted power flow by the amount that was previously flowing through the interconnecting line. On the other hand, the stationary short-circuit current i_4 (after ~25 ms) through the breaker of line WF-S is almost halved (12 kA instead of 25 kA) and a breaker of lower rating may be chosen.

The emphasis in this very simple example is not on the numeric values of these currents, but rather on the qualitative observation that results from network splitting into sub-networks. By selecting a network topology that is only weakly meshed at some locations and contains sub-networks, fast interruption or limiting devices at connecting locations can prevent that short circuit contributions from one subsystem feed into another. This may significantly reduce the requirements of other protection devices. Whether slower devices with an interruption time of only 25 ms (to interrupt the stationary currents) are acceptable in the first place remains a crucial point. Maybe the fault can now be cleared by de-energizing the sub-network completely [22], either by control of the converter terminals or in support with AC side CBs. A discussion of this issue is beyond the scope of this work.

V. Discussion and Conclusion

It is evident that the rate of rise and the amplitude of the transient and stationary part of the fault current through a breaker are extremely demanding due to the low resistance of the network. None of the existing breaker technologies is optimum with respect to fault clearing time, maximum interruption capability, losses during normal operation, and costs. The concept used in AC network, namely placing a CB at the end of each line, cannot be used in HVDC networks. Also the concept that is used today in point-to-point connections, opening the AC side breakers to de-energize the system, is not foreseeable for larger DC networks. We have thus reported on some other options that have an influence on the amplitude or the rate of rise of the short-circuit current to reduce the requirements on DC-CBs. Some of them address the problem inherently, others by adding components.

A reduction of the DC side filter capacitors would result in an inherent reduction of the amplitude of the first peak of the transient short-circuit current. However, accepting a larger ripple on the DC network or choosing another converter technology cannot be based on fault clearance considerations alone. Similarly for the grounding scheme of the network: besides the influence on mainly the stationary fault current, arguments with respect to converter terminal operation and insulation coordination have to be considered. As was explained in section III, the choice of CB technology is today mainly a trade-off between speed and on-state losses. No single one solution is optimum for the entire network, but from knowing the possible prospective short-circuit currents, it may be possible to select a different technology at different locations in the network. One might accept the high losses at certain strategic locations where fast breaker action is inevitable.

As was mentioned before, de-energizing the complete network in the case of a fault will not be acceptable. However, one may be forced to accept a partial network outage as long as no suitable CBs are available. One may choose the network topology in a way that it can be split into sub-networks. Such a network is not as densely meshed as desired, but the losses from a few fast CBs at the connecting links may be accepted and the faulty sub-network can then be shut down to clear the fault.

In summary, the discussion on choosing an acceptable fault clearing option is not only driven by the CB technology, but may even involve the selection of converter terminal technology or the network topology.

The simulations in the present contribution concentrated only on the fault current through the breaker, but of course also the current through the freewheeling diodes and other sensitive components should be looked at in future studies. Moreover, in this study we modeled all nodes identically; even the offshore connection. The studies should be repeated with more detailed converter models as soon as a concrete location for the first network is known.

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