A new empirical large-signal model of Si LDMOSFETS for high-power amplifier design

Article *in* IEEE Transactions on Microwave Theory and Techniques · October 2001

Impact Factor: 2.24 · DOI: 10.1109/22.942576 · Source: IEEE Xplore

4 authors, including:

Jaehyok Yi

19 PUBLICATIONS **461** CITATIONS

SEE PROFILE

A New Empirical Large-Signal Model of Si LDMOSFETs for High-Power Amplifier Design

Youngoo Yang, *Student Member, IEEE,* Young Yun Woo, Jaehyok Yi, and Bumman Kim, *Senior Member, IEEE*

***Abstract*—We propose a new empirical large-signal model of silicon laterally diffused MOSFETs for the design of various modes of high-power amplifiers. The new channel current model has only nine parameters that represent the unique operation principles of a MOSFET. In the channel current model, we include the thermal phenomena of high-power devices. To accurately characterize high-power devices, we incorporate the channel heating and heat-sink heating effects by providing two thermal capacitances and two thermal resistances. Nonlinear capacitances, including deep subthreshold and triode regions, as well as normal saturation regions, are extracted and modeled. For validation of our model, a 1.4-GHz 5-W amplifier is implemented, and the measured and simulated results match very well.**

***Index Terms*—Empirical large-signal model, high-power amplifier, LDMOSFET.**

I. Introduction

THE silicon RF laterally diffused MOSFETs (LDMOSFETs) have become the most popular devices for high-power amplifiers of the base stations and the relay equipments for wireless communication systems. Due to fast evolving device technology, LDMOSFETs with more than 150-W peak envelope power (PEP) at a frequency band of third-generation wireless systems have been already reported [1], [2]. Therefore, researchers are highly motivated to develop a large-signal model to effectively design high-power amplifiers that use silicon LDMOSFETs.

Previously, the empirical channel current models, based on closed-form analytic expressions, were reported by Miller *et al.* (Motorola model) [3] and Angelov *et al.* (Chalmers model) [4] and have shown further good results [3]–[8]. Nevertheless, the channel current model we propose in this paper has advantages, i.e., it requires fewer parameters to fully describe the normal I–V curve of RF LDMOSFET (nine parameters excluding parameters expressing self-heating effects). Each parameter represents the unique characteristics of the I–V curve, with little interdependence. There are no denominators, tuning exponents as a fitting parameter, and series expansion functions in the proposed channel current model.

Manuscript received October 25, 2000; revised December 23, 2000. This work was supported by the Agency of Defense Development and by the Korean Ministry of Education under the BK21 Project.

The authors are with the Department of Electronic and Electrical Engineering, Microwave Application Research Center, Pohang University of Science and Technology, Namgu Pohang 790-784, Korea, (email: alice@postech.ac.kr).

Publisher Item Identifier S 0018-9480(01)07589-5.

For high-power amplifiers, thermal phenomena are very important due to a high rise in temperature, thus, a large-signal model for high-power devices must properly include self-heating effects. To extract the accurate temperature-dependent model parameters, I–V curves are measured under several bias conditions: using short-pulsed (SP) gate biases with a pulsewidth of 1 μs at several ambient temperatures (34 °C, 54 °C, 74 °C, 94 °C, and 114 °C), long-pulsed (LP) biases with a pulsewidth of 2 ms at room temperature (34 °C), and dc. $R_{\rm th}$ is extracted from the channel heating and $C_{\rm th}$ is extracted from the transient response. DC I–V measurements at room temperature are also carried out to extract $R_{\rm th,H}$ for the heat-sink effect. To simplify the measurement, drain biases are dc for all the measurements.

For validation of the model, the measured and modeled I–V curves using SP, LP, and dc are compared. The measured and modeled S-parameters are also shown. Finally, an 1.4-GHz 5-W class-AB amplifier is designed and implemented. The measured third-order intermodulation (IM3) and power-added efficiency (PAE) are compared with the simulated ones, resulting in good agreement.

II. Large-Signal Model of LDMOSFETs

Fig. 1 shows equivalent circuits with a low-pass thermal circuit to represent the self-heating effect. The thermal circuit has additional thermal resistance ($R_{\rm th,H}$) and capacitance ($C_{\rm th,H}$), which describe the heat-sink effect. This model has nonlinear drain pad capacitance $C_{\rm dd}$ and pad-to-substrate series resistance $R_{\rm dd}$, which adds a lossy substrate effect to the well-known nonlinear capacitances $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm ds}$.

The linear components and package parasitics are extracted by a simultaneous S-parameter fitting with the measured S-parameter sets at four different points on a two-dimensional I–V plane, with external G_m's and $R_{\rm ds}$'s directly extracted from the measured SP I–V curves [9]. The four points are selected on the expected large-signal load line, as shown in Fig. 2. The extracted model parameters for Ericsson's RF LDMOSFET PTF10107 are shown in Table I.

A. Channel Current Model

The channel current model proposed in this paper has closed-form analytic equations and continuously expresses the

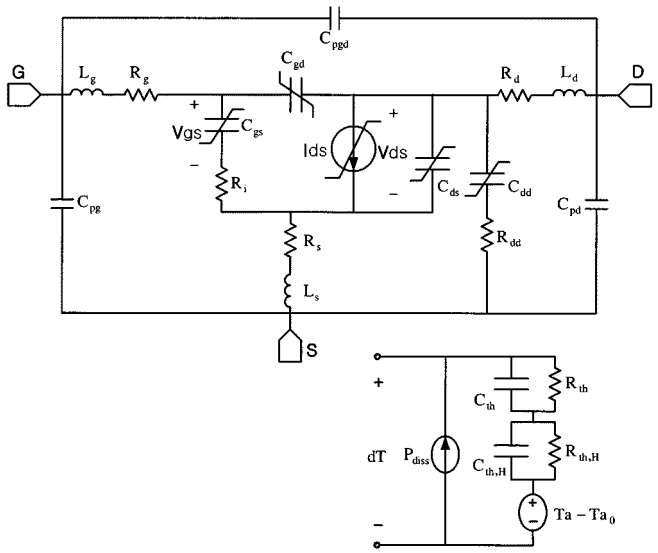


Fig. 1. Equivalent circuits for silicon LDMOSFET with a thermal circuit including heat-sink effect.

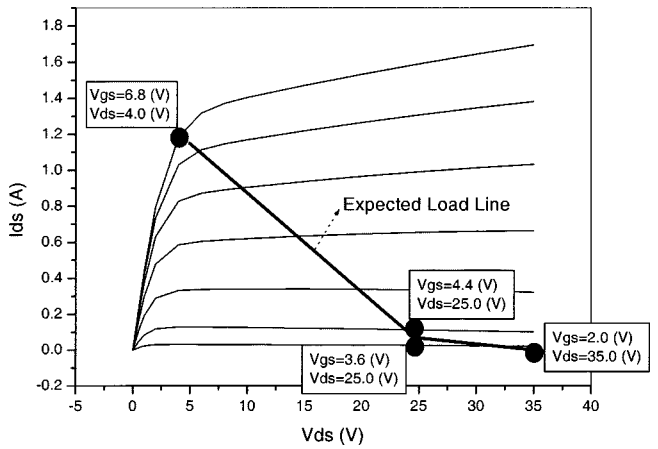


Fig. 2. Selected four points on the expected large-signal load line to extract linear and parasitic components.

operation mode change of the silicon MOSFET. Expression for a new channel current model is given by

$$V_{\rm sat} = V_{\rm gs} - S_c \cdot \ln\left[1 + \exp\left(\frac{V_{\rm gs} - S_v}{S_c}\right)\right] \quad (1)$$

$$V_T = T_v + \theta \cdot V_{\rm ds} \quad (2)$$

$$V_{\rm eff} = V_{\rm sat} - V_T \quad (3)$$

$$V_{gm} = \frac{T_c}{2} \cdot \ln\left[1 + \exp\left(\frac{2 \cdot V_{\rm eff}}{T_c}\right)\right] \quad (4)$$

$$\alpha_{\rm H} = \alpha \cdot \left[1 - \tanh\left(\gamma \cdot V_{\rm eff}\right)\right] \quad (5)$$

$$I_{\rm ds} = \beta \cdot V_{gm} \cdot \tanh\left(\alpha_{\rm H} \cdot V_{\rm ds}\right) \cdot \left(1 + \lambda \cdot V_{\rm ds}\right) \quad (6)$$

where α and γ are the parameters that determine the shapes of channel current saturation through the drain voltages, λ is the parameter to express the channel length modulation, and θ explains the threshold voltage variation according to the drain

TABLE I
EXTRACTED LINEAR AND PARASITIC COMPONENTS OF SILICON RF LDMOSFET, PTF10107

Parameter	Value	Unit
R_g	3.87E-1	Ω
R_d	1.1E-5	Ω
R_s	3.9E-2	Ω
L_g	7.92E-1	nH
L_d	8.28E-1	nH
L_s	3.7E+1	pH
C_{pg}	3.4E-1	pF
C_{pd}	3.1E-1	pF
C_{pgd}	4.13	fF
R_i	4.06E-1	Ω
R_{dd}	3.81E+1	Ω
τ	25.46	ps

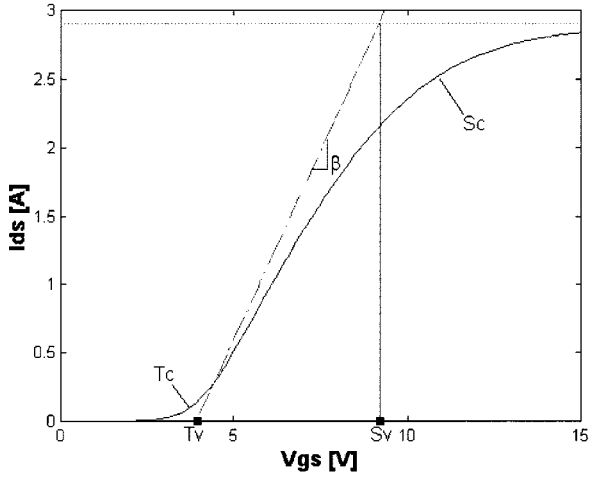


Fig. 3. Calculated channel current behavior versus gate voltage ($V_{\rm gs}$) for PTF10107 at $V_{\rm ds} = 25$ V, ambient temperature $= 34\,^{\circ}$C, and SP measurement.

voltages. The other five parameters express the channel current transient versus the gate voltages. The general channel current behavior of MOSFETs versus $V_{\rm gs}$ is shown in Fig. 3. The curve in Fig. 3 is extracted from the proposed channel current model $V_{\rm gs}$ dependencies. In this figure, the operational modes of MOSFETs are the subthreshold, linear, and saturation regions, which are characterized by functional behavior. The parameter T_v (threshold voltage) demarcates the transition region between the subthreshold and linear, and the parameter S_v (saturation voltage) demarcates the region between linear and saturation. The parameter T_c (threshold curvature) determines the curvature shape of the subthreshold to the linear region transition, the parameter S_c (saturation curvature) determines the curvature shape of the linear to the saturation region transition, and the parameter β determines the channel current slope at the linear

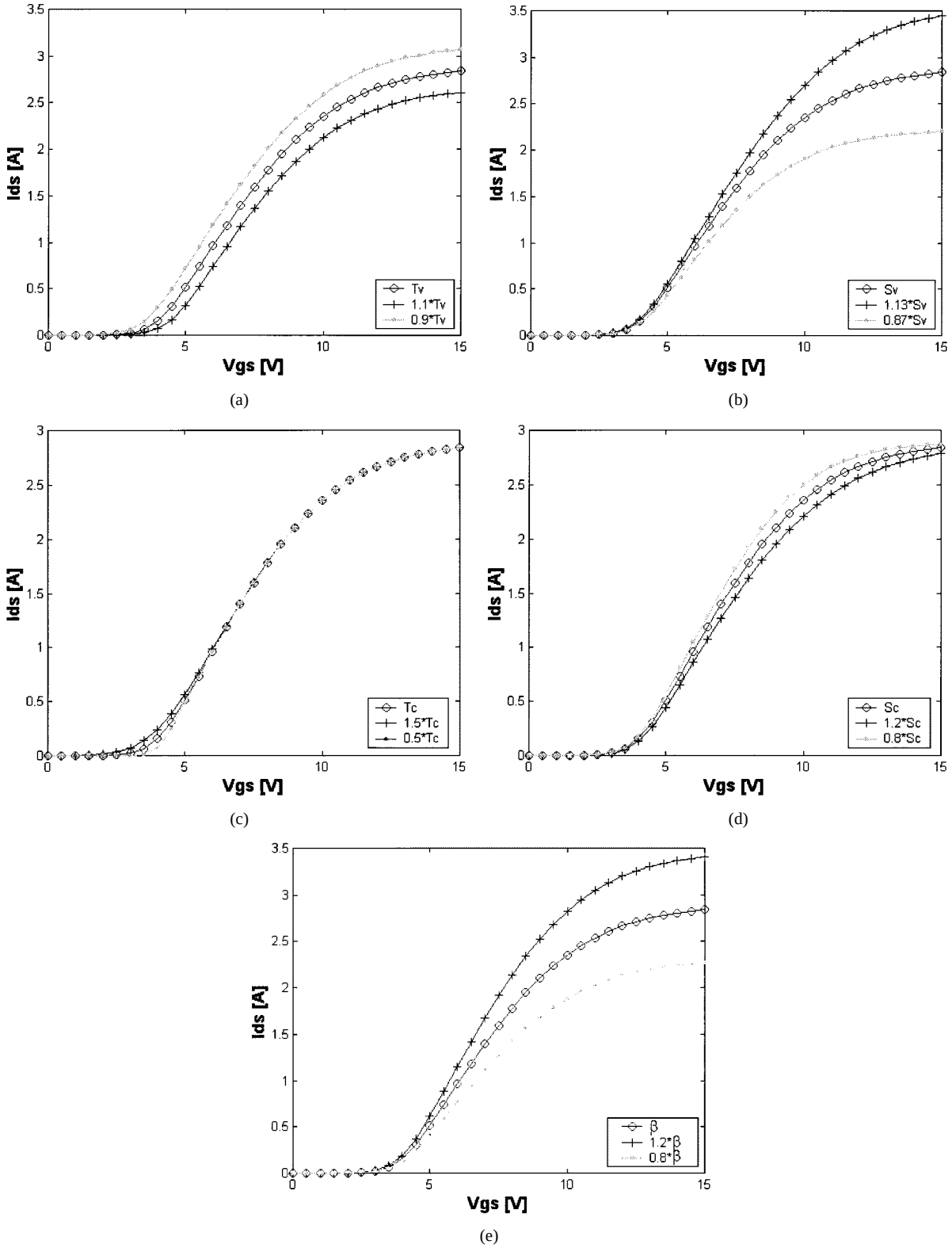


Fig. 4. Calculated channel current variation versus gate voltage (V_{gs}) with varying parameter values for: (a) T_v, (b) S_v, (c) T_c, (d) S_c, and (e) β.

region. Fig. 4 shows the characteristic variations of the channel current with changing parameter values. Each parameter has a unique role to describe the channel current, with little interdependence between them. Due to the clear role of each parameter, we can intuitively obtain the initial values of parameters, which are very close to the final solutions. Therefore, the optimization procedure, to just trim the initial values, is very fast and always converges the final wanted values.

The threshold voltage and effective mobility are sensitive to the junction temperature [10], [11]. Hence, we take T_v and β to be the temperature-dependent parameters, which are depicted in the following equations, using tangent hyperbolic functions to

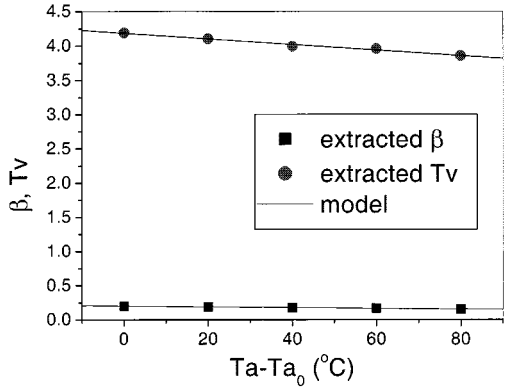


Fig. 5. Fitted results of the temperature-dependent channel current parameters.

provide range restriction (i.e., always positive) to the parameters:

$$T_v = T_{v_0} \cdot \left[1+\tanh\left(T_{v_1} \cdot dT + T_{v_2}\right)\right] \tag{7a}$$

$$\beta = \beta_0 \cdot \left[1+\tanh\left(\beta_1 \cdot dT + \beta_2\right)\right] \tag{7b}$$

$$dT = \begin{cases} T_a - T_{a_0}, & \text{for pulsed } I\text{–}V \text{ with } SP \\ R_{\rm th} \cdot P_{\rm diss} + T_a - T_{a_0}, & \text{for pulsed } I\text{–}V \text{ with } LP \\ (R_{\rm th} + R_{\rm th,H}) \cdot P_{\rm diss} + T_a - T_{a_0}, & \text{for DC } I\text{–}V \end{cases} \tag{8a}$$

$$P_{\rm diss} = I_{\rm ds} \cdot V_{\rm ds} \tag{8b}$$

where dT in (8a) represents a rise in channel temperature due to an ambient temperature variation $(T_a - T_{a_0})$ for SP I–V. For LP I–V, dT represents a rise in channel temperature due to a channel heating by power dissipation and an ambient temperature variation $(R_{\rm th} \cdot P_{\rm diss} + T_a - T_{a_0})$. For dc I–V, dT represents a rise in channel temperature due to channel and heat-sink heatings by power dissipation and an ambient temperature variation $((R_{\rm th} + R_{\rm th,H}) \cdot P_{\rm diss} + T_a - T_{a_0})$.

The temperature-dependent parameters are extracted to fit the SP I–V measurement data at various ambient temperatures (34 °C, 54 °C, 74 °C, 94 °C, and 114 °C in this experiment). The extracted data are fitted as functions of the channel temperature rise, using (7a) and (7b). The fitting results are shown in Fig. 5 and the extracted channel current parameters are shown in Table II. The measured and modeled SP I–V curves are compared in Fig. 6.

B. $R_{\rm th}$ and $C_{\rm th}$ Extraction

Section II-A modeled the thermal dependence of the channel current at different ambient temperatures without a self-heating effect. Next, $R_{\rm th}$ and $C_{\rm th}$ extractions are performed to complete (7) and (8). $R_{\rm th}$ can be directly extracted by comparing the channel current model, which is extracted by the measured SP I–V with the measured LP I–V data. LP measurements with a pulsewidth of 2 ms model the channel heating caused by thermal resistance of the channel $(R_{\rm th})$, and can successfully exclude the heat-sink heating caused by thermal resistance of the heat sink $(R_{\rm th,H})$ because the thermal time constant of the high-power silicon LDMOSFETs is generally below a few hundreds of microseconds and the thermal time constant of the heat sink is very large compared to the pulsewidth.

TABLE II
EXTRACTED CHANNEL CURRENT PARAMETERS OF SILICON RF LDMOSFET, PTF10107

Parameter		Value	Unit
Sv		9.158	V
Sc		1.953	V
Tv	Tv_0	7.362	V
	Tv_1	-7.02E-4	
	Tv_2	-4.62E-1	
Tc		8.82E-1	V
θ		1.12E-2	
α		7.61E-1	V^{-1}
γ		1.85E-1	V^{-1}
λ		1.52E-1	V^{-1}
β	β_0	5.064	Ω^{-1}
	β_1	-1.62E-1	
	β_2	-1.598	

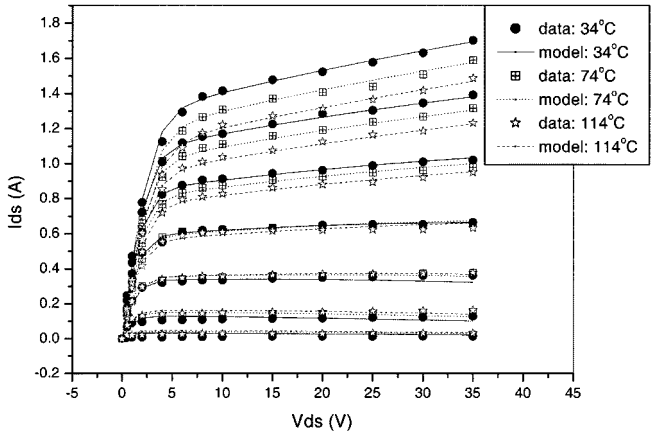


Fig. 6. Measured and modeled SP I–V at different ambient temperatures: $V_{\rm gs} = 3.6$–8.4 V, step $= 0.8$ V.

The following is an $R_{\rm th}$ extraction routine using the channel current model $(I_{\rm ds_{model}})$ with temperature-dependent parameters from Section II-A:

$$I_{\rm ds_{data,LP}} = I_{\rm ds_{model}}\left(dT_{\rm data,LP}\right) = I_{\rm ds_{model}}\left(R_{\rm th}, P_{\rm diss,data,LP}\right) \tag{9}$$

where

$$\begin{cases} dT_{\rm data,LP} = R_{\rm th} \cdot P_{\rm diss,data,LP} + T_a - T_{a_0} \\ T_a - T_{a_0} = 0 \\ P_{\rm diss,data,LP} = V_{\rm ds_{data,LP}} \cdot I_{\rm ds_{data,LP}}. \end{cases}$$

$P_{\rm diss,data,LP}$ (the measured channel power dissipation) can be obtained from the measured LP channel current, which is symbolized as $I_{\rm ds_{data,LP}}$. In (9), the only unknown parameter is $R_{\rm th}$, which is extracted from the measured LP channel current and

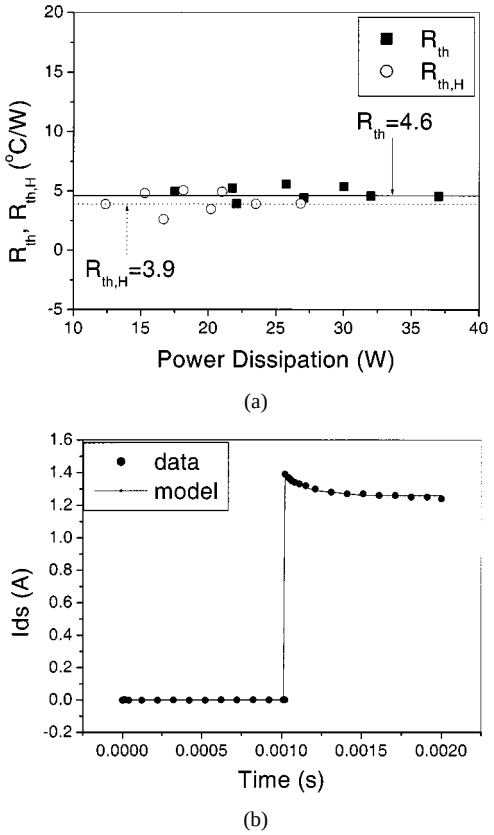


Fig. 7. Silicon LDMOSFET, PTF10107. (a) Extracted $R_{\rm th}$ and $R_{\rm th,H}$. (b) Measured and modeled transient responses.

the model at different channel power dissipations by an iteration method.

The $C_{\rm th}$ is optimized to fit the measured transient response to the channel current model. In the same way, $R_{\rm th,H}$ can be extracted by comparing the channel current model with the measured dc I–V data. The $C_{\rm th,H}$ was not extracted and can be assumed as a large value (in this experiment, one) because the heat sink has a very large thermal time constant compared to the channel. The extracted $R_{\rm th}$ and $R_{\rm th,H}$ of the silicon LDMOSFET, PTF10107 are shown in Fig. 7(a). The measured and optimized transient responses at $V_{\rm gs} = 8.4$ V and $V_{\rm ds} = 10$ V are shown in Fig. 7(b). The representative $R_{\rm th}$ is 4.6 (°C/W) and the optimized $C_{\rm th}$ is 3.55E-5. The extracted $R_{\rm th,H}$ in this experiment is 3.9 (°C/W). The thermal time constant of the channel becomes 163.3 μs. Consequently, the measured and modeled SP, LP, and dc I–V curves at 34 °C are shown in Fig. 8.

C. Nonlinear Capacitance Model

We extracted and modeled nonlinear capacitances of the silicon LDMOSFETs, including the deep subthreshold and triode regions, which are very important for class-AB, class-B, or class-C operation. The nonlinear capacitances are $C_{\rm gs}$ (gate–source capacitance), $C_{\rm gd}$ (gate–drain capacitance), $C_{\rm ds}$ (drain–source capacitance), and additionally $C_{\rm dd}$ (drain–substrate capacitance). Each capacitance is extracted from the measured S-parameters at various bias points, and modeled using continuous single empirical functions. The functions of

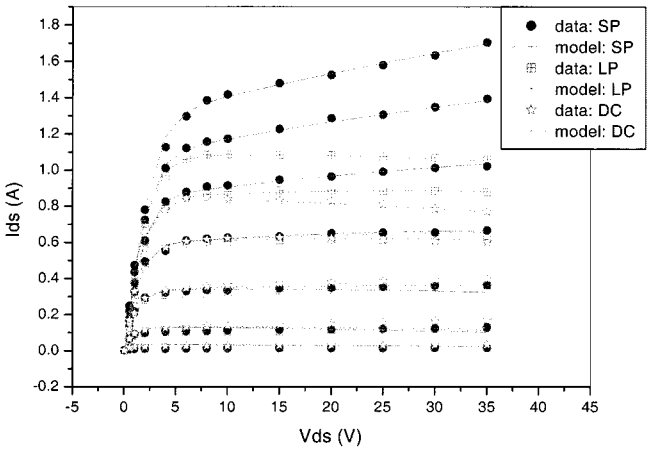


Fig. 8. Measured and modeled SP, LP, and dc I–V curves at 34 °C: $V_{\rm gs} = 3.6$–8.4 V, step $= 0.8$ V for SP I–V, $V_{\rm gs} = 3.6$–7.6 V, step $= 0.8$ V for LP I–V, and $V_{\rm gs} = 3.6$–6.8 V, step $= 0.8$ V for dc I–V.

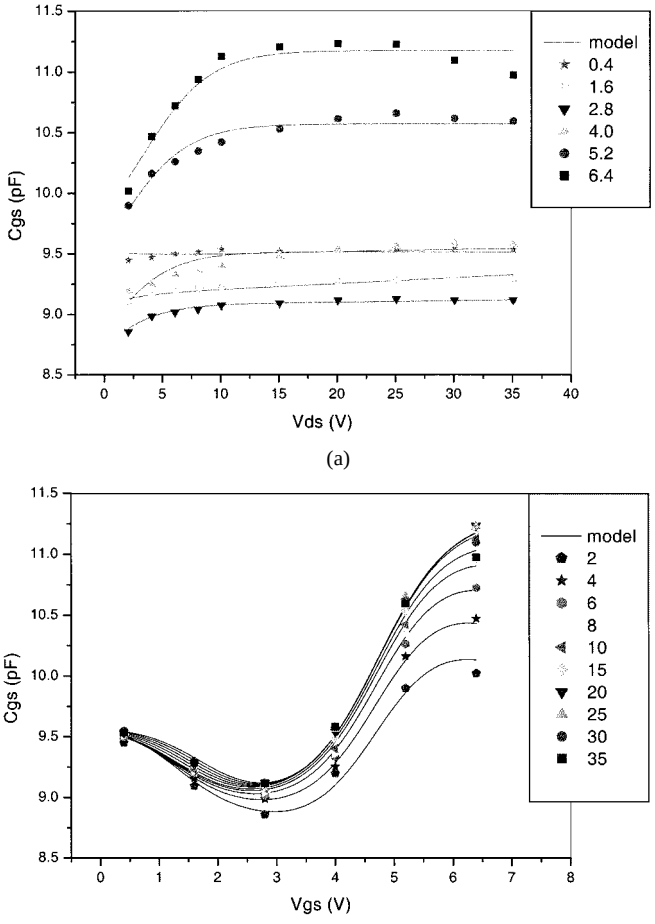
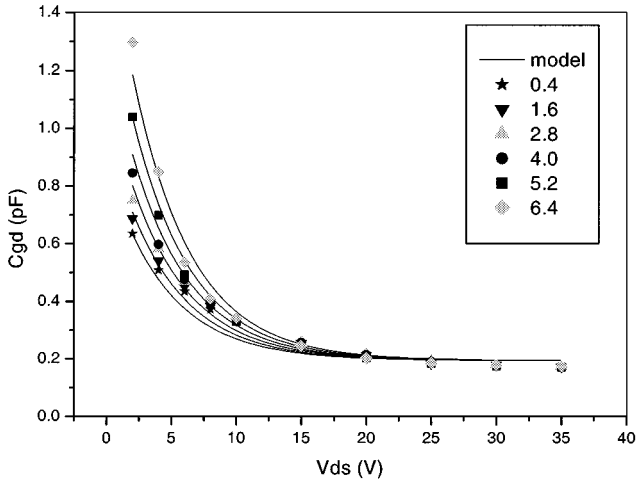


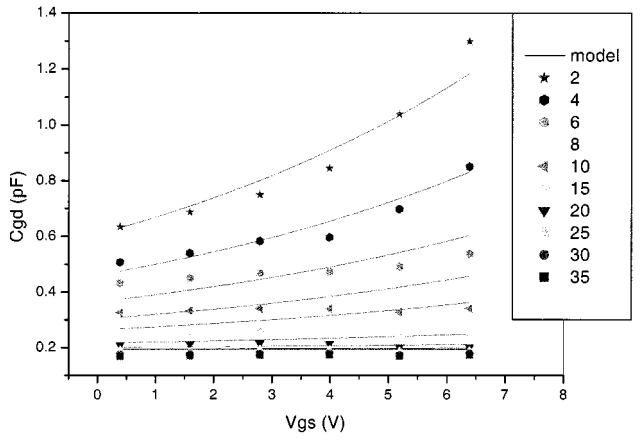
Fig. 9. Extracted and modeled $C_{\rm gs}$ for: (a) $V_{\rm gs} = 0.4$–6.4 V and (b) $V_{\rm ds} = 2$–35 V (lines: model, points: data).

nonlinear capacitances used in this modeling are as follows:

$$C_{\rm gs} = a_0 + a_1 \cdot \Big[\tanh\left(a_2 \cdot V_{\rm gs} + a_3\right) + a_4 \cdot \tanh\left(a_5 \cdot V_{\rm gs} + a_6 \cdot V_{\rm ds} + a_7\right)\Big] \cdot \tanh\left(a_8 \cdot V_{\rm ds} + a_9 \cdot V_{\rm gs} + a_{10}\right) \quad (10)$$



(a)



(b)

Fig. 10. Measured and modeled $C_{\rm gd}$ for: (a) $V_{\rm gs} = 0.4$–6.4 V and (b) $V_{\rm ds} = 2$–35 V (lines: model, points: data).

$$C_{\rm gd} = b_0 + b_1 \cdot \left[1 + \tanh\left(b_2 \cdot V_{\rm gs} + b_3\right)\right] \cdot \ln\left[1 + \exp\left(\frac{b_4 \cdot V_{\rm ds} - b_5}{b_6}\right)\right] \tag{11}$$

$$C_{\rm ds} = c_0 + c_1 \cdot \left[1 + \tanh\left(c_2 \cdot V_{\rm ds} + c_3\right)\right] \tag{12}$$

$$C_{\rm dd} = d_0 + d_1 \cdot \left[1 + \tanh\left(d_2 \cdot V_{\rm ds} + d_3\right)\right]. \tag{13}$$

Fig. 9 shows the extracted and modeled $C_{\rm gs}$ versus $V_{\rm ds}$ in Fig. 9(a) and $V_{\rm gs}$ in Fig. 9(b). Drain and gate bias dependences of $C_{\rm gs}$ are accurately extracted and modeled using (10). The extracted data show a very smooth and continuous trend. Extracted and modeled nonlinear $C_{\rm gd}$ are shown in Fig. 10, which are modeled as a function of $V_{\rm ds}$ [see Fig. 10(a)] and $V_{\rm gs}$ [see Fig. 10(b)], which also show very strong bias dependences. Nonlinear $C_{\rm ds}$ and $C_{\rm dd}$ are modeled with only $V_{\rm ds}$ dependence. The results are shown in Figs. 11 and 12, respectively. The modeled and extracted nonlinear capacitances are in very good agreement throughout the whole large-signal operating region. The model parameters of the nonlinear capacitances are presented in Table III.

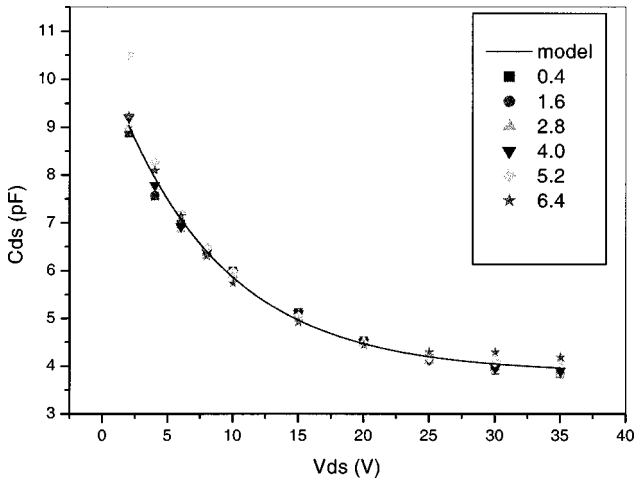


Fig. 11. Measured and modeled $C_{\rm ds}$: $V_{\rm gs} = 0.4$–6.4 V (lines: model, points: data).

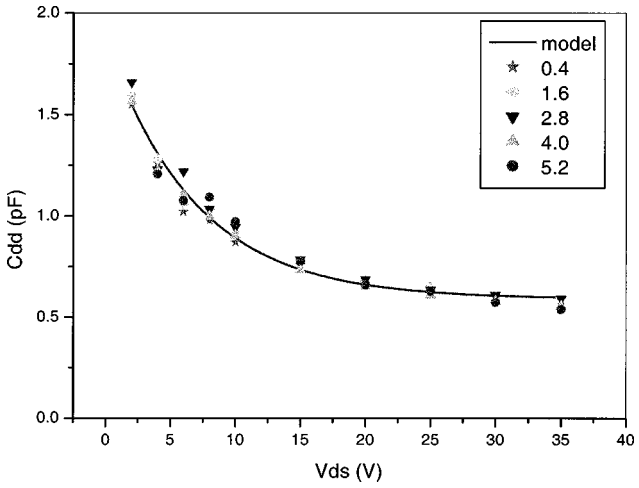


Fig. 12. Measured and modeled $C_{\rm dd}$: $V_{\rm gs} = 0.4$–5.2 V (lines: model, points: data).

III. Experimental Verification

This large-signal model is implemented in Agilent's ADS, using symbolic defined device (SDD). The measured and modeled S-parameters at $V_{\rm gs} = 4.4$ V and $V_{\rm ds} = 25$ V, which is a quiescent bias point of class-AB operation, are given in Fig. 13. It shows a very good agreement. The measured and modeled I–V curves shown in Fig. 6 (SP I–V curves) and Fig. 8 (SP, LP, and dc I–V curves) are also in good agreement. To accurately consider the bias-dependent self-heating effect, it is very important for the model to accurately fit the measured SP I–V curves, as well as LP and dc I–V curves.

For verification of the model, a 1.4-GHz class-AB hybrid power amplifier has been designed and implemented using harmonic-balance simulation in ADS. An amplifier schematic diagram is shown in Fig. 14. A 3.9-Ω series chip resistor and a 500-Ω shunt chip resistor are used to enhance the stability factor and the gate bias feeding. Source impedance $(Z_{\rm S})$, excluding the series and shunt resistors, is $5.6 - j1.7$. The load impedance $(Z_{\rm L})$ is $5.2 + j1.0$. Fig. 15 shows the measured and simulated output power, IM3 power, and PAE when two-tone input (1.4-

TABLE III
MODEL PARAMETERS OF NONLINEAR CAPACITANCES OF LDMOSFET, PTF10107

Capacitance	Parameter	Value	Capacitance	Parameter	Value
C_{gs} (pF)	a_0	9.278	C_{gd} (pF)	b_0	0.194
	a_1	-1.177		b_1	4591.45
	a_2	-0.812		b_2	6.85E-2
	a_3	3.84		b_3	-2.763
	a_4	-0.738		b_4	-2.531
	a_5	-0.324		b_5	46.154
	a_6	0.174		b_6	11.46
	a_7	1.519	C_{ds} (pF)	c_0	3.863
	a_8	-1.67E-2		c_1	1192.3
	a_9	0.956		c_2	-5.95E-2
	a_{10}	-1.116		c_3	-2.947
			C_{dd} (pF)	d_0	187.684
				d_1	-93.5497
				d_2	7.294E-2
				d_3	2.489

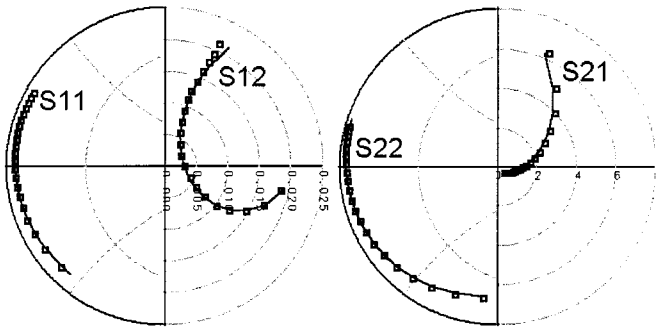


Fig. 13. Measured and modeled S-parameters at $V_{\rm gs} = 4.4$ V, $V_{\rm ds} = 25$ V, and frequency $= 0.6$–3.3 GHz.

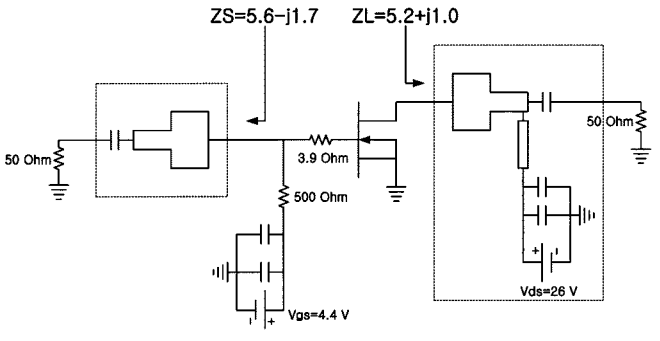


Fig. 14. Schematic of the implemented class-AB amplifier.

and 1.401-GHz, 1 –MHz spacing) is applied. At 1-dB gain compression point, the average output power is 34.8 dBm and the PAE is 33.3% for two-tone input. The measured and simulated IM3s match very well throughout the input drive level. The good agreement between them indicates the accuracy of our model.

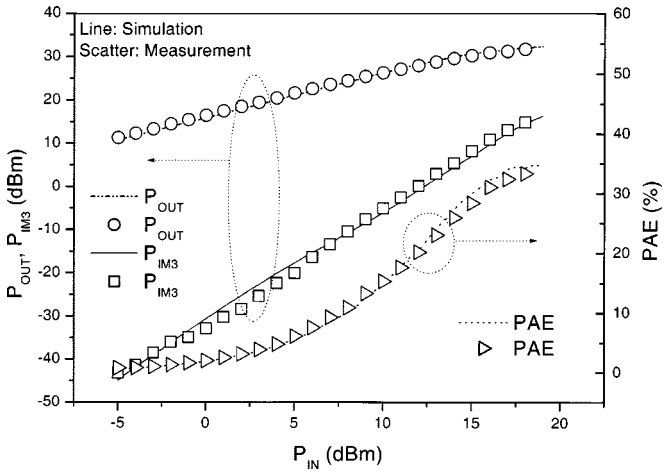


Fig. 15. Measured and simulated output power, IM3, and PAE characteristics of the 1.4-GHz class-AB amplifier for two-tone test (1.4- and 1.401-GHz, 1-MHz spacing).

IV. CONCLUSIONS

To design a high-power class-AB or class-B amplifier, a behavioral (or empirical) large-signal model for silicon LDMOSFET has been proposed. The new channel current model has fewer parameters than those previously reported, as well as minimized interdependence among the parameters, no tuning exponents as a fitting parameter, no denominators, and no series-expansion functions. This model also has the capability to express the thermal behaviors of the device and heat sink. The related parameters are extracted from the measurement of SP, LP, and dc I–V curves. The SP and LP measurements are performed by applying pulsed bias to the gate and dc bias to the drain, which requires a very simple measurement setup compared to dual-pulsed measurements.

An $R_{\rm th}$, $R_{\rm th,H}$, and $C_{\rm th}$ extraction routine, using the measured SP, LP, and dc I–V curves through various power dissipations and transient response, has been explained. Nonlinear capacitances are extracted and modeled using continuous empirical functions, including the deep subthreshold and triode regions, which is important to predict the large-signal behavior of the high-power amplifier that operates under class AB.

To verify the model, a 1.4-GHz class-AB power amplifier has been designed and implemented. The measured and simulated amplifier characteristics of output power, IM3, and PAE are very closely matched. Hence, the proposed behavioral large-signal model will be very useful in the design of high-power amplifiers at various classes of operation.

REFERENCES

[1] A. Wood, W. Brakensiek, C. Dragon, and W. Burger, "120 Watt, 2 GHz, Si LDMOS RF power transistor for PCS base station applications," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1998, pp. 707–710.

[2] C. P. Dragon, W. R. Burger, B. Davidson, E. Krvavac, N. Dixit, and D. Joersz, "High power RF-LDMOS transistors for wireless communication base station applications," in *MWE'99 Microwave Workshop Dig.*, 1999, pp. 289–294.

[3] M. Miller, T. Dinh, and E. Shumate, "A new empirical large signal model for silicon RF LDMOSFET's," in *IEEE MTT-S Technol. Wireless Applicat. Dig.*, 1997, pp. 19–22.

[4] I. Angelov, N. Rorsman, J. Stenarson, M. Garcia, and H. Zirath, "An empirical table-based model," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 2350–2357, Dec. 1999.
[5] W. R. Curtice, J. A. Pla, D. Bridges, T. Liang, and E. E. Shumate, "A new dynamic electro-thermal nonlinear model for silicon RF LDMOSFET's," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1999, pp. 419–422.
[6] D. Heo, E. Chen, E. Gebara, S. Yoo, J. Larskar, and T. Anderson, "Temperature dependent MOSFET RF large signal model incorporating self heating effects," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1999, pp. 415–418.
[7] L. Bengtsson, I. Angelov, H. Zirath, and J. Olsson, "An empirical high-frequency large-signal model for high-voltage LDMOS transistors," in *28th European Microwave Conf. Dig.*, 1998, pp. 733–738.
[8] Y. Chen, C. Huang, C. Weng, and B. Liew, "Characteristics of deep-submicrometer MOSFET and its empirical nonlinear RF model," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 611–615, May 1998.
[9] Y. Yang, J. Yi, and B. Kim, "Accurate RF large signal model of LDMOSFET's including self-heating effect," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 387–390, Feb. 2001.
[10] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*. New York: McGraw-Hill, 1987.
[11] P. Perugupalli, M. Trivedi, K. Shenai, and S. K. Leong, "Modeling and characterization of an 80 V silicon LDMOSFET for emerging RFIC applications," *IEEE Trans. Electron Devices*, vol. 45, pp. 1468–1478, July 1998.

Youngoo Yang (S'99) was born in Hamyang, Korea, in 1969. He received the B.S. degree in electronic engineering from Han-Yang University, Ansan, Korea, in 1997, and is currently working toward the Ph.D. degree at the Pohang University of Science and Technology (POSTECH), Namgu Pohang, Korea.

His research interests include linearization techniques and behavioral modeling of high-power amplifiers, large-signal modeling of the microwave devices, and radio-frequency integrated-circuit (RFIC) design.

Young Yun Woo was born in Taegu, Korea, in 1976. He received the B.S. degree in electronic and electrical engineering from Han-Yang University, Seoul, Korea, and is currently working toward the M.S. degree at the Pohang University of Science and Technology (POSTECH), Namgu Pohang, Korea.

His current research interests include RF power-amplifier design and linear power amplifier (LPA) control circuits design.

Jaehyok Yi was born in Taegu, Korea, in 1974. He received the B.S. and M.S. degrees in electronics and electrical engineering from the Pohang University of Science and Technology, Namgu Pohang, Korea, in 1997 and 1999, repectively, and is currently working toward the Ph.D. degree in the electronics and electrical engineering at the Pohang University of Science and Technology.

His research interests include the design and simulation of the behavior of linear RF power amplifiers.

Bumman Kim (S'77–M'78–SM'97) received the Ph.D. degree in electrical engineering from Carnegie-Mellon University, Pittsburgh, PA, in 1979.

From 1978 to 1981, he was engaged in fiber-optic component research at GTE Laboratories Inc. In 1981, he joined the Central Research Laboratories, Texas Instruments Incorporated, where he was involved in development of GaAs power FETs and monolithic microwave integrated circuits (MMICs). He has developed a large-signal model of a power FET, dual-gate FETs for gain control, and high-power distributed amplifiers, and various millimeter-wave MMICs. In 1989, he joined the Pohang University of Science and Technology (POSTECH), Namgu Pohang, Korea, where he is currently a Professor in the Electronic and Electrical Engineering Department and Director of the Microwave Application Research Center, where he is involved with device and circuit technology for MMICs. He has authored or co-authored over 100 technical papers in this area.

Dr. Kim is a member of the Korean Academy of Science and Technology.