High-Performance Front-End Converter for Avionics Applications

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Abstract - Front-end converters of future 400 Hz aircraft power systems will be expected to meet rigorous specifications, including low total harmonic distortion (THD<10%) and low electromagnetic interference (EMI), with small size and high efficiency. This paper identifies an active-clamped isolated SEPIC converter suitable for such applications. Zero-voltage-switching accomplished by the active clamp and a single-layer transformer design boost the converter efficiency to 90%. An accurate averaged switch model is developed for this converter which shows that its dynamics are simpler than that of a conventional SEPIC and thus better suited for closed-loop controller design. THD of less than 5% has been achieved with average current control.

I. INTRODUCTION

Future commercial aircraft will require high performance isolated front-end converter for supplying power to loads such as in-flight entertainment systems, communications, and navigation equipment. High performance implies low total harmonic distortion (THD) of the 400 Hz input current, as well as high efficiency, over a wide range of operating voltages and line frequencies. A SEPIC rectifier is a good choice for such applications because of the ease of isolation and the presence of an input filter inductor. However, the SEPIC rectifier suffers from the disadvantages of low efficiency and damping or snubbing requirement. Addition of an active voltage clamp overcomes some of these disadvantages. The active clamp [1-5] as well as the SEPIC rectifier [6-9] are well known and implemented in the industry. It is shown in this paper how an active-clamped SEPIC rectifier can meet the rigorous requirements of avionics application. In particular, a method of approximate analysis of the active-clamped SEPIC is developed. An averaged switch model suitable for simulations is also derived and experimentally verified. Finally, a high-performance SEPIC rectifier that achieves efficiency greater than 90% and THD less than 5% is demonstrated.

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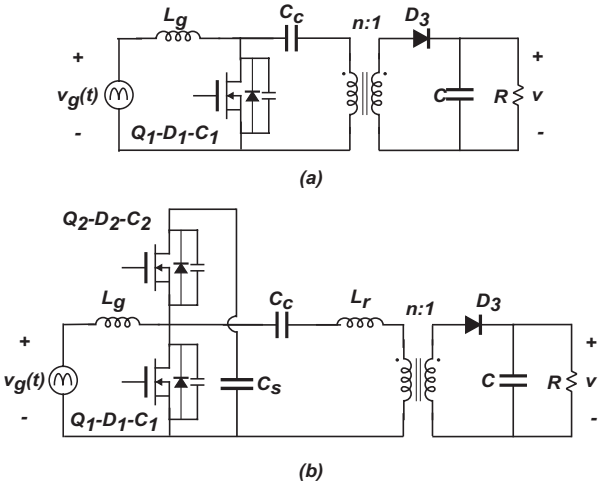


Fig. 1 Performance of a conventional SEPIC rectifier (a) is improved by adding an active voltage clamp (b).

A. 400 Hz system requirements

The airborne electrical equipment is classified under various categories depending on the types of input and output. The dc output level is typically 14 V or 28 V and can have a floating battery with a significant capacity. The input can either be single phase or three phase, 115 Vac or 230 Vac, and at a constant or variable frequency. The constant frequency is 400 Hz, while the variable frequency has two ranges, either 360 to 650 Hz or 360 to 800 Hz. The nominal input-voltage variation range is small, but the abnormal voltage variation can be ± 15%. In addition, the 115 V equipment must withstand voltage surges up to 170 V and as low as 70 V. This is further complicated by the fact that the input could go to zero for a duration up to 200 ms. For a front-end converter, this requirement implies that a large energy storage capacitor must be incorporated. This converter is thus required to operate satisfactorily over a wide range of operating points.

Table 1: Harmonic limits

Harmonic number	Limit (% of 1st)
Odd non-triplen (n=5,7,..,37)	30/n
Odd triplen (n=3,9,..,39)	15/n
Even (n=2,4)	1/n
Even (n=6,8,..,40)	0.25

The system that is considered for this work assumes a single-phase input voltage from 90 V to 135 V in the 360 to 800 Hz category; the nominal being 115 V at 400 Hz. The output voltage is 28 V without a floating battery and supplies a 100 W load.

One particular harmonic standard sets a limit on the line current harmonics as listed in Table 1. Generally the first few odd triplen and odd non-triplen harmonics dominate the frequency spectrum. This means that a total harmonic distortion of less than 10% is required. To provide an adequate design margin, we have set a target of THD less than 5% for this project.

B. The SEPIC rectifier

A CCM SEPIC rectifier was chosen for this project for the following reasons:

a. Single-stage design with ease of isolation between input and output.
b. Buck-boost conversion ratio that enables arbitrary output voltage and design flexibility.
c. Low device stresses as compared to isolated boost topologies.
d. Small EMI filter requirement compared to flyback and other DCM approaches.
e. Startup and inrush currents are limited. This is crucial where the hold-up time requirement is up to 200 ms as in this application and a large output capacitor is required.

The SEPIC has been implemented in numerous ways as a PFC rectifier at 60Hz, and good performance has been reported [6-9]. It has been also implemented with soft switching e.g. ZCT, ZCS or auxiliary commutation and in DCM as well as in boundary conduction mode (BCM). The overall reported efficiencies, which vary with the load, are in the range of 70 to 85%. The reported THDs are in the range of 5 to 20% while the reported power factors span 0.92 to 0.99.

A conventional SEPIC suffers from the following disadvantages:

a. Switching losses of the transistor due to hard switching and reverse recovery of the output diode.
b. Increased voltage stresses on the transistor due to energy in the transformer leakage inductance; needs a snubber.
c. Serious losses in the transformer due to proximity effect resulting in low efficiency.
d. Difficulty of optimizing transformer construction.
e. Need for damping of the coupling capacitor to stabilize the current loop in the case of average current control.

C. Improving SEPIC performance

An active voltage clamp added to the SEPIC allows the utilization of transformer leakage inductance to achieve soft switching and simultaneously limits the peak voltage stress on the transistor. A controlled current slope of the output diode minimizes its reverse recovery and related losses. Zero-voltage switching of both the transistors curtails the switching losses. This enables the converter to operate with higher switching frequencies. High switching frequency, in turn, causes reduction in the size of reactive components and allows for higher controller bandwidth and lower THD. It is also discovered that the control-to-input current transfer function is well behaved such that damping of the coupling capacitor is not required.

A good transformer construction contributes to the achievement of high efficiency. With non-optimal windings, the proximity losses are very substantial. Interleaving of the windings can reduce the maximum MMF between the conductors and thus the proximity loss; however, the phase difference between the primary and secondary currents reduces the benefits of interleaving. With single-layer windings, the proximity losses are greatly reduced. The solution employed here was to design the power stage of SEPIC such that single-layer windings could be employed in the transformer. This approach implies that the magnetizing inductance is relatively small. In turn, this suggests that the transformer could also assist in obtaining zero-voltage switching.

D. Outline of discussion

In order to improve the SEPIC performance by the active clamp, a complete analysis of the converter is required. This paper explains an easy and distinct way of analysis of active-clamped SEPIC converter, based on approximation of the resonant waveforms to rectilinear waveforms. This method, explained in Section II, is very important for averaged-switch modeling of active-clamped converters. Design of the rectifier is covered in Section III. A converter model suitable for computer simulations is developed in Section IV and Appendix A. Sections V and VI present simulation and measurement results of this rectifier. A detailed PSpice netlist is listed in Appendix B.

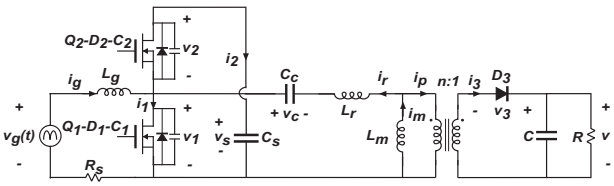


Fig. 2 Definition of converter currents and voltages

II. STEADY STATE ANALYSIS

A. Actual steady-state operation

The actual waveforms of the leakage inductance current (i_r) and the clamp voltage (v_s) of the converter of Fig. 2 are shown in Fig. 3. The conducting devices are also shown corresponding to the six intervals in a switching period. The main transistor-diode combination conducts for time dT_s, where d is the duty cycle and T_s is the switching period. Interval 1 is the time when D_1 conducts and Q_1 has to be turned on with ZVS. Similarly Q_2 is turned on with ZVS shortly after interval 4 when current in D_2 is still positive. During interval 5, the current in the leakage inductance reverses, and discharges C_1 during interval 6.

Another operating mode, called as DCM of the active-clamped converters, has not been taken into account in this paper. This mode, in which L_m has a large current ripple and assists in the zero voltage switching of Q_1, is analyzed in [4].

B. Approximations

A method based on approximations is justified in the engineering domain if it is simple, sufficiently accurate, and insightful. An example is that of the small ripple approximation in converters. Such approximations make the converter analysis a simple task.

For this converter, we approximate the resonant waveforms to rectilinear waveforms. As seen in Fig.4, the resonant transitions of the converter waveforms are ignored i.e. the intervals *3*,*4* and *6* are neglected as they are small compared to the switching period. In other words, in comparison with Fig.3, the waveforms in Fig.4 have only three intervals, which are the intervals 1,2 and 5 of Fig.3. The interval 1 is for a period xT_s , T_s being the switching period, and is much smaller than that projected in the Fig. 4. The intervals 1 and 2 make up dT_s, where d (duty cycle) is the control variable. It can be construed that while d is the primary side duty cycle, d'_x can be called as the secondary side duty cycle of the diode. The resonant transition intervals can not be ignored if they become comparable to the conduction intervals of the switches, i.e. when the switching frequency is very high.

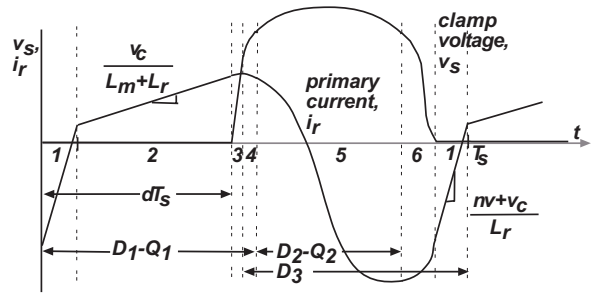


Fig. 3 Detailed steady-state waveform of the clamp voltage and primary current corresponding to Fig. 2. The conducting devices are also shown

The clamp voltage, v_s, is assumed to be constant which also means that the resonant frequency of the L_r-C_c-C_s tank is smaller than the switching frequency. It is possible to take into account the resonant waveforms of i_r and v_s and write the averaged equations but for a greater simplicity, this resonance is neglected.

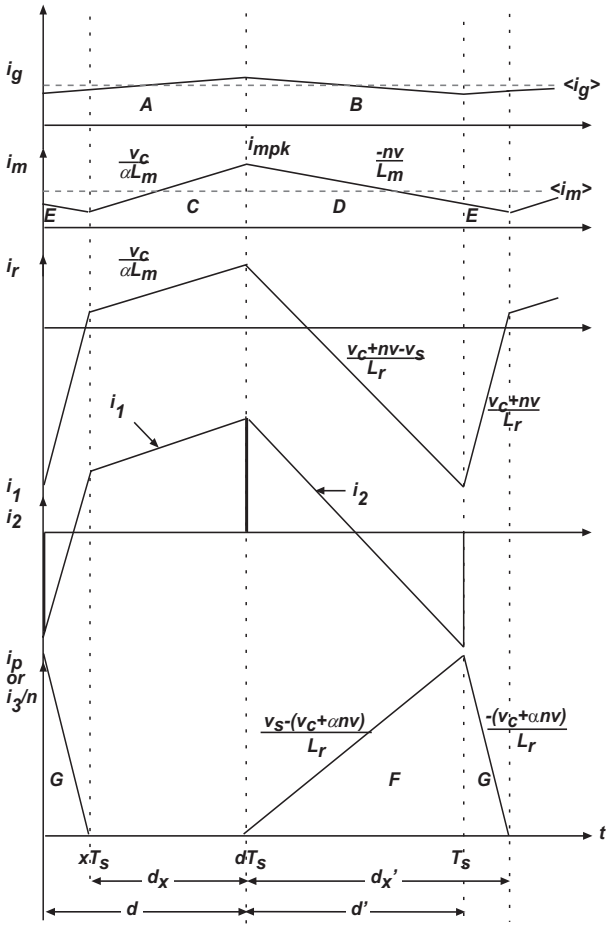


Fig. 4 Approximated waveforms

C. Conversion ratio and ZVS condition

To find the steady-state dc-dc conversion ratio, usual inductor volt-second balance and capacitor charge balance are performed on the respective elements. The volt-second balance on L_g and L_m gives the following two equations

$$V_s = \frac{V_g}{D'}, \tag{1}$$

$$M = \frac{nV}{V_g} = \frac{D - X}{D' + X}\frac{1}{1+\beta}, \tag{2}$$

Charge balance on the output capacitor, i.e. equating the average diode current to the load current, gives

$$M = \frac{n^2 R T_s}{2L_r}\left(D' + X\right)\left(1 - D - MD'\left(1+\beta\right)\right), \tag{3}$$

Eliminating X from the above, we get the quadratic,

$$\left(\frac{2L_r\left(1+\beta\right)}{n^2 R T_s}\right)M^2 + \left(\frac{2L_r}{n^2 R T_s} + D'\left(1+\beta\right)\right)M - D = 0, \tag{4}$$

Solving for M and rearranging the terms, we obtain

$$M = \frac{D}{D'}\frac{1}{\left(1+\beta\right)}\frac{2}{\left(1 + \frac{K}{D'} + \sqrt{\left(1+\frac{K}{D'}\right)^2 + \frac{4KD}{D'^2}}\right)}, \tag{5}$$

where

$$K = \frac{2L_r \,\|\, L_m}{n^2 R T_s}, \tag{6}$$

We also get an expression for the duty cycle in terms of the conversion ratio as follows.

$$D = \frac{\left(1+\beta\right)M}{1+\left(1+\beta\right)M}\left(1 + K + K\left(1+\beta\right)M\right), \tag{7}$$

This expression allows us to predict the duty ratio variation over the line cycle when the required conversion ratio M is known.

From a state-plane diagram of the resonance between L_r and C_r (the resonant capacitance or the equivalent device output capacitance), a condition for zero voltage switching of Q_1 is found. It is expressed as:

$$f_0 \geq \frac{f_s}{\pi}\cdot\frac{\sqrt{(1+2M)D' - D}}{D'(D - MD')}, \tag{8}$$

where f_s is the switching frequency and f_0 is the tank resonant frequency.

III. RECTIFIER DESIGN

To verify the operation of the converter and to test the accuracy of the approximations made in Section II, a prototype converter (Fig. 6) is designed and built. Quasi-static approximation, which allows us to treat each point of the line cycle as a steady state dc-dc operating point, is assumed initially. The analysis for this converter assumes the same operating mode for each operating point. Each point has a specific input voltage, input current, intermediate capacitor voltages, average inductor currents and equivalent load while the output voltage and the actual load are constant. Analysis of the operating points is done, using a spreadsheet, to understand the duty cycle variation, ZVS possibility, percentage current ripple and peak voltages etc.

The turns ratio of the transformer determines the voltage stresses inflicted on the switching devices. It can either be selected to meet a pre-selected device voltage rating, as in this case where a Schottky diode is intended on the output side, or to meet current ratings on the input or output side. Once the turns ratio is fixed, the RMS, average and peak currents can be calculated. Approximate expressions for RMS currents, based on the conventional SEPIC rectifier operation, are given below. The duty cycle for the active-clamped SEPIC is higher than a conventional SEPIC for the same conversion ratio, hence the actual RMS currents will be approximately 10% higher than those calculated from the following expressions.

$$I_{Q1.rms} = I_{ac.rms}\sqrt{1 + \frac{8}{3\pi}\frac{V_M}{nV}}, \tag{9}$$

$$I_{Q2.rms} = I_{ac.rms}\,\frac{4V_M}{3nV}\sqrt{\frac{1}{2} + \frac{1}{4\pi}\frac{nV}{V_M}}, \tag{10}$$

Once the active devices are selected and their output capacitances are known, the equivalent capacitance C_r of the resonant tank is determined. The resonant tank, formed between C_r and L_k, is responsible for zero voltage switching of Q_1 and Q_2. It is figured out, from the ZVS condition (8), that it is not possible to achieve ZVS over the entire line cycle. This is not a problem because the switching loss is high near the peak and whether the converter switches with ZVS or not near the zero crossings hardly affects the total loss savings.

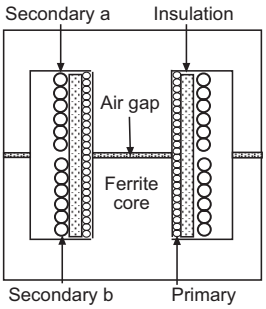


Fig. 5 Single-layer transformer construction

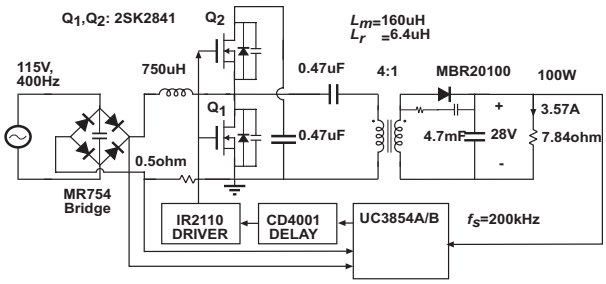


Fig. 6 Power stage design and suggested control scheme

A large input inductor value effectively filters out switching ripple and can reduce the EMI filter size. On the other hand, a small input inductor improves the dynamic response, required to reduce the zero crossing distortion. This value can be selected by setting a certain limit on the value of peak ripple current, for example 20% of $\langle i_g \rangle$ at the peak.

The value of the magnetizing inductance has to be small enough for the purpose of a single-layer transformer construction. Small value means a large current ripple, which is acceptable in this case as the converter operation is different than a conventional SEPIC. A suggested design condition to select the value of magnetizing inductance is that the current ripple at θ=45° operating point of the line cycle should be about 100%. This enables the magnetizing inductance to aid in the ZVS of Q_1 near the zero crossings. An example of the transformer construction is given in Fig.5. The secondary a and secondary b windings are connected in parallel. A low flux density (0.1 to 0.15 T) should be chosen for the transformer to minimize the core losses. A thick insulation between the windings is used to obtain desired leakage inductance. A core with a long window length and a small window area is perfectly suitable for a single-layer construction. A PQ3535 core is used in this case but a smaller EC41 core can also be used.

The value of the clamp capacitor is chosen so that its resonant frequency with L_r is less than the switching frequency to justify the rectilinear waveform approximation. The coupling capacitor is selected similarly.

The switching frequency is selected to be 200 kHz. As the switches are configured in a half-bridge, it is easy to drive them with a commercially available half-bridge driver IC such as IR2110. It is important to control the delay between the switching of the two transistors. While the delay for the transition from Q_1 to Q_2 is not critical, the delay, when Q_1 switches on with ZVS, is critical. This delay is practically fine-tuned because the tolerances in the leakage inductance, device capacitance and parasitic elements involved can significantly affect the ZVS condition. The delay is implemented with NOR logic and RC circuits.

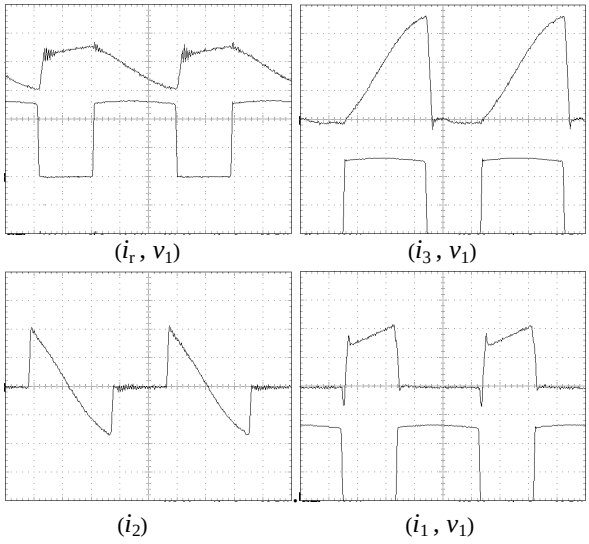


Fig. 7 Measured waveforms of the dc-dc converter verify the operation and support the approximations made. The time base is 1us/div.

A high-performance current error amplifier is needed for the average current control because of the 400 Hz application. One such amplifier, with GBW = 5 MHz and a low offset, is available in the UC3854A/B enhanced power factor preregulator that is used in the rectifier prototype.

The measured waveforms of the prototype rectifier, operated with open loop at dc input, are shown in Fig. 7. It can be seen that the diode's reverse recovery has been minimized with the use of Schottky diode. A low loss snubber is put across the output diode to limit its peak voltage stress. It is verified that zero-voltage-switching is accomplished. The transformer losses are also found to be small. The measured efficiency at 115 V dc input and a load of 100 W is 93%.

IV. CONVERTER MODELING

Averaged switch modeling is a simple and fast approach of modeling a wide variety of converters with different control schemes. In this method, the converter switching elements, which are non-linear and generate switching harmonics, are segregated as illustrated in Fig. 8, and their terminal waveforms are averaged over a switching period. The averaging process removes the switching harmonics from the converter waveforms, resulting in a large-signal, time-invariant averaged model. The switches are replaced by dependent sources in the model. The values of these sources are expressed in terms of other independent inputs to the switch network. The inputs to the switch network include control inputs, independent voltages and currents of the switch network and in some cases, external voltages and currents in the converter.

With the definition of the switch network as in Fig.8, our averaged switch model is based on averaging the waveforms shown in Fig.4. The averaging process is complicated in terms of the algebra involved but nevertheless is easy to visualize. Appendix A describes the process in detail. The result is a set of equations that can be manipulated to express certain terminal quantities in terms of the others and the control input. Out of the six terminal quantities defined, at least three have to be independent. The averaged quantities $\langle i_1 \rangle$, $\langle v_2 \rangle$ and $\langle i_3 \rangle$ are carefully selected to be expressed as functions of $\langle v_1 \rangle$, $\langle i_2 \rangle$, $\langle v_3 \rangle$ and external control input d. The '$\langle\rangle$' sign denotes averaging of the waveform over a switching period. Although the quantities could be interchanged without affecting the model behavior, ease of simulation is mainly considered for selecting $\langle i_1 \rangle$, $\langle v_2 \rangle$ and $\langle i_3 \rangle$ as dependent quantities. It can be seen that the independent quantities $\langle v_1 \rangle$, $\langle i_2 \rangle$, $\langle v_3 \rangle$ can easily be estimated from the dc state to be V_g, 0 and V respectively.

A careful modeling approach as investigated in [14] must be followed for the active-clamped converters as well. As seen in Fig. 4, in the waveform of i_r or i_3/n, there happens to be one interval of conduction other than dT_s and $d'T_s$. The length of this interval is denoted as x, and is similar the diode conduction interval of conventional discontinuous conduction mode converters. The length of this interval could be computed by equating the peak currents obtained from the two slopes of the waveform of i_r. However, this would imply that the average voltage of the leakage inductance is zero. This in turn leads to a reduced-order model that does not accurately predict the high frequency dynamics. However, if this mistake is carried forward to derive the averaged model, the analysis becomes simpler. The resulting model has equations for the dependent variables only in terms of the independent variables of the switch network, which makes it self-reliant. Such a model could be used for analysis of the low-frequency dynamics. Nonetheless, we have observed substantial discrepancies between the observed experimental waveforms and the predictions of this simplified model. In particular, the predicted $\langle i_3 \rangle$ waveform differs significantly.

A more accurate method is to find the value of x by equating the average leakage inductor current $\langle i_r \rangle$ to the area under the waveform of i_r. In the present case, it is easier to find the average output diode current $\langle i_3 \rangle$ and equate it to the area under the waveform of i_3. The derivation of the model equations is given in Appendix A. The complete averaged circuit model of the converter is obtained by replacing the switch network with the controlled sources given by (17), (35) and (36) as seen in Fig. 9. All other elements are the same as in the original converter circuit. This averaged circuit model is used with a circuit simulator such as PSpice. As shown in the next sections, a good agreement with the experiment is attained with this more accurate model.

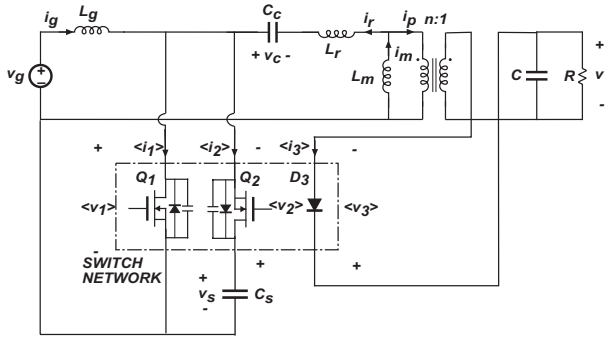


Fig. 8 Defining switch network and terminal quantities for the active-clamped SEPIC

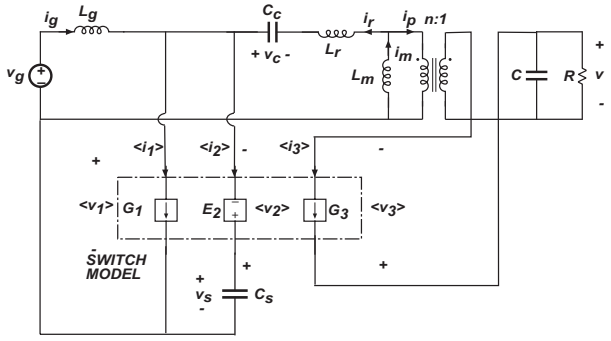


Fig. 9 Replacement of the switch network by dependent sources governed by the model equations

V. SIMULATIONS WITH PSPICE

The averaged switch model equations are implemented in PSpice as shown in Appendix B. The experimental prototype has the exact values of components as seen in the schematic or the netlist. The simulations are performed step by step to understand the converter operation. First, the dc-dc conversion ratio, input and output currents, intermediate voltages and power balance are verified at different duty cycles. Next, the small-signal transfer functions such as control-to-output, control-to-input and line-to-output transfer functions are plotted with the help of ac analysis. The Bode plots are verified by experimental measurement. The control-to-input current transfer function, called as $G_{id}(s)$, is simulated at an operating point of $\theta = 45°$ of the line cycle assuming quasi-static approximation. The simulated and measured transfer functions agree very well as seen in Fig. 10. It is noticed that the dip in phase, just before 10 kHz, goes to a minimum at the operating point corresponding to the peak of the line cycle. The transfer functions are also plotted by varying each reactive component over a certain range to see its effect on the dynamics. Such a method is inevitable because it is very difficult to get an insightful analytical expression for the poles and zeros of such transfer functions for this converter. However, it can be deduced that the high frequency asymptote of $G_{id}(s)$ is $\frac{V_s}{sL_g}$. It is also found that $G_{id}(s)$ is very well behaved as compared to that of a conventional SEPIC as seen in Fig. 11. It can be seen that in contrast with the SEPIC exhibiting undamped complex poles and zeros, the active-clamped SEPIC exhibits a very smooth response.

When simulated with open loop, we can find small-signal transfer functions, such as the control-to-input current transfer function, for various operating points

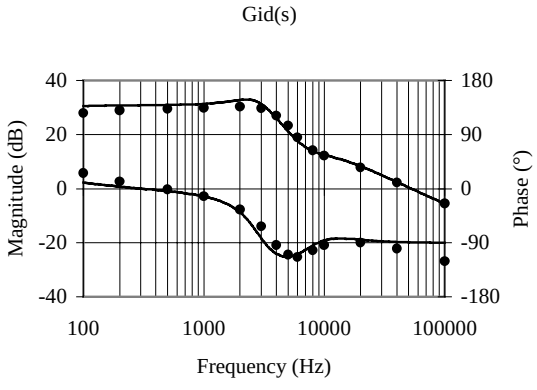


Fig. 10 Control-to-input current transfer function Simulated (dark) and measured (dots) Magnitude (top) and phase (bottom) Operating point : Vg=115 V, V=28 V, P=100 W

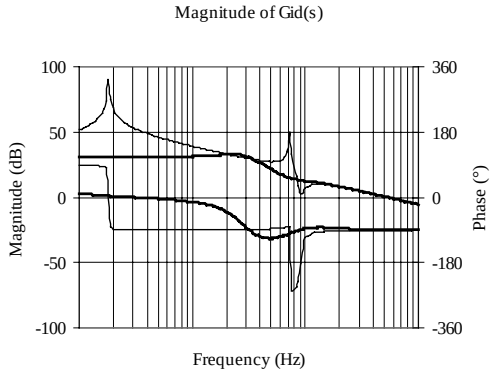


Fig. 11 Comparison of Gid(s) of SEPIC (light) and active-clamped SEPIC (dark)

over the line cycle. Each operating point will have a set of values of input voltage, input current, capacitor voltages, output current and the equivalent load but a fixed output voltage as if the rectifier operated as a dc-dc converter. This is really the quasi-steady state operation in which the converter dynamics are fast enough so that each set of operating values over the line cycle is satisfied. However, if the dynamics are slow, the intermediate capacitor voltages and inductor currents may not follow the ideal operating points. The violation of quasi-steady state may or may not lead to instabilities in the converter.

The current loop of the rectifier is compensated based on $\theta = 45°$. It must be ensured that the loop gain is sufficient at 400 Hz and the crossover frequency is high. A simple PI controller with high frequency roll-off is used in the feedback. The simulated loop gain is shown in Fig. 12. The crossover frequency, at 75 kHz, is expected to be sufficiently accurate as the magnitude responses from simulations and experiment match very closely in Fig.10. The predicted phase margin from

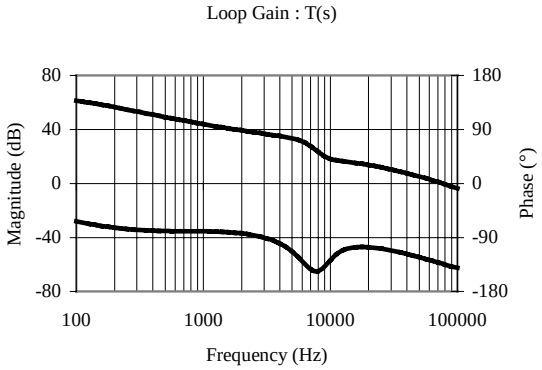
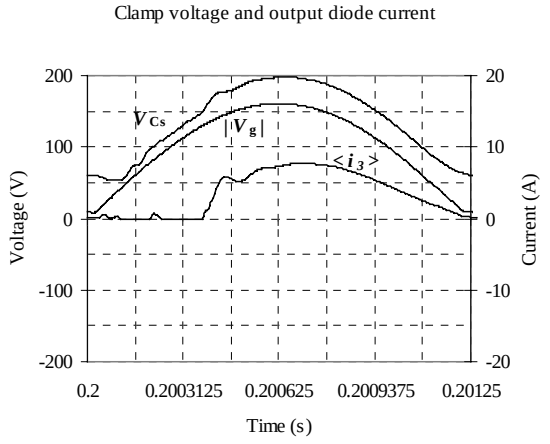
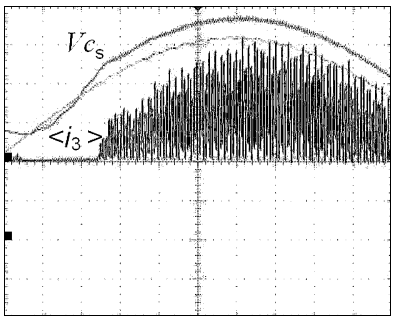


Fig. 12 Loop gain magnitude and phase for θ=45° operating point

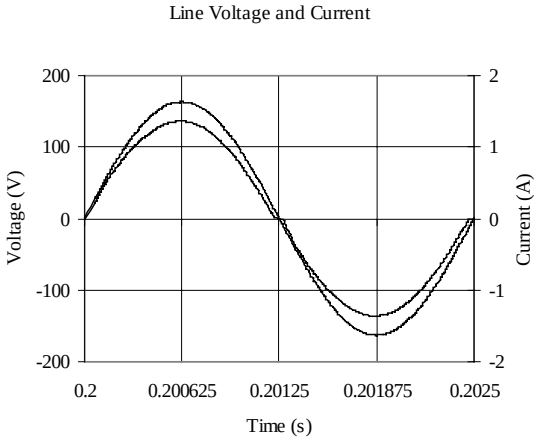


(a) Simulation

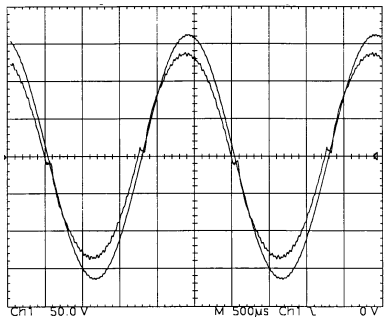


(b) Experiment

Fig. 13 Clamp voltage (offset by 100 V) at 50 V/div, and output diode current at 5 A/div with reference to the rectified line voltage.



(a) Simulation



(b) Experiment

Fig. 14 Line voltage (outer) and line current (inner). Scale for experimental: 50 V/div and 0.5 A/div. THD for (a) = 0.8%, THD for (b) = 3%

simulation is 50° at that particular operating point. The θ = 90° operating point is also found to be stable with the above compensation. It should be once again noted that even if one point is stable in terms of loop dynamics, the stability of the converter as whole depends on the validity of quasi-static approximation.

The closed-loop transient operation is simulated next. The simulated line voltage and line current are given in Fig.14 (a). It can be seen that they match very well with the experimental measurements in Fig.14 (b). The problems with convergence of the simulator during transient analysis have to be patiently dealt with. Some tricks like writing the model equations in different ways, setting node voltages and initial conditions and carefully choosing the time step help in convergence. With such simulations, it must be verified that various voltages and currents in the converter vary as expected over the line cycle. In some cases, the internal quantities may exhibit abnormal operation even if the final answer, for e.g. waveform of the line current, is correct. It is observed that the output diode current is zero for a certain time in the beginning of the line cycle. The clamp capacitor waveform also does not vary ideally, as it should, based on the quasi-static approximation. Both the observations are confirmed by simulations as seen in Fig. 13.

VI. EXPERIMENTAL RESULTS

As explained towards the end of Section III, a converter prototype showed the desired power stage performance and helped in verifying the approximate averaged switch model. The rectifier was then implemented with average current control. Standard issues like isolation of the primary side ground and housekeeping power supply have not been considered in this paper. The EMI filtering is not a serious problem because of the inherent input filtering and high switching frequency. The measured THD is in fact very small over the line frequency range of 400 Hz to 800 Hz.

The converter operates satisfactorily over the wide line frequency range. The measured efficiency of the converter varies from 90% to 88% over the same range. The THD varies a little around 3%. The THD is

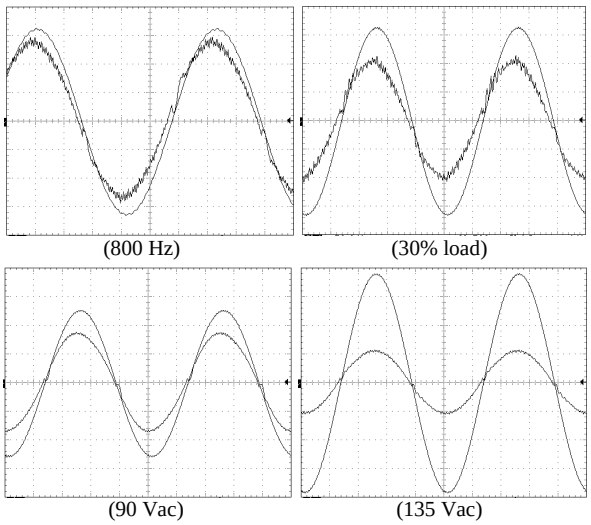


Fig. 15 Line voltage (outer) and line current (inner) for different conditions

Table 2

Test condition	Efficiency %	THD %
800Hz	88.8	3.2
30% load	91.0	4.8
90Vac	88.5	4.1
135Vac	90.2	2.6

improved from 4-5% to 3% by adding a 6.8V zener diode to clamp the output of the current error amplifier of UC3854B. The converter has been also tested at low line and high line as well as at reduced load. The summary of results is given in Fig. 15 and Table 2.

VII. CONCLUSIONS

A high-performance rectifier suitable for 400 Hz avionics application has been identified and demonstrated. A SEPIC converter has been modified by adding the well-known active voltage clamp to improve its performance. The rectifier has a total harmonic distortion of less than 5% over a wide line frequency variation. The measured efficiency of 90% is quite high for an isolated SEPIC based topology. A new approach for averaging of approximate waveforms in the converter and active clamp snubber circuit is proposed; this approach allows derivation of a tractable equivalent circuit that can be easily implemented in computer simulators. The averaged switch model accurately predicts the rectifier small-signal transfer functions and transient response. Experimental results confirm the accuracy of this proposed model. In addition, it is noted that the assumptions inherent in the quasi-static approximation are not satisfied by the experimental prototype.

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APPENDIX A

Derivation of the model equations

From the waveforms in the adjacent figure, we can now write the averages of the terminal voltages and currents of the switch network as follows:

$$\langle v_1 \rangle = d' \langle v_s \rangle , \tag{11}$$

$$\langle v_2 \rangle = d \langle v_s \rangle , \tag{12}$$

$$\langle v_3 \rangle = (d - x)\left(\frac{\langle v_C \rangle}{\alpha n} + \langle v \rangle \right), \tag{13}$$

where $\alpha = 1 + \beta = 1 + \dfrac{L_r}{L_m}$

To find the value of *x*, we can write the equation for average output current

$$\langle i_3 \rangle = \frac{n}{2} \frac{\left(\langle v_s \rangle - \left(\langle v_c \rangle + \alpha n \langle v \rangle \right) \right)}{L_r} d' T_s \left(d' + x \right), \tag{14}$$

simplifying (14), we get

$$d' + x = \frac{\langle i_3 \rangle R_e}{n} \frac{1}{\left(\langle v_1 \rangle - d' \left(\langle v_c \rangle + \alpha n \langle v \rangle \right) \right)}, \tag{15}$$

where,

$$R_e = \frac{2L_r}{T_s}, \tag{16}$$

Thus by substituting the value of (*d*-*x*) from (15) back in (13), we get,

$$\langle i_3 \rangle = \frac{n\left(\langle v_1 \rangle - d' \left(\langle v_c \rangle + \alpha n \langle v \rangle \right) \right)}{R_e} \left(1 - \frac{\alpha n \langle v_3 \rangle}{\langle v_c \rangle + \alpha n \langle v \rangle} \right), \tag{17}$$

It remains to find the expressions for $\langle i_1 \rangle$ and $\langle i_2 \rangle$. We can write the node equations for the currents as follows,

$$i_p = i_m - i_r , \tag{18}$$

$$i_1 = i_g + i_r - i_2 , \tag{19}$$

We first have to find the areas A to G of the switching intervals as defined in Fig. 16. We can then write

$$\langle i_1 \rangle = A + C + E - G , \tag{20}$$

$$\langle i_2 \rangle = B + D - F , \tag{21}$$

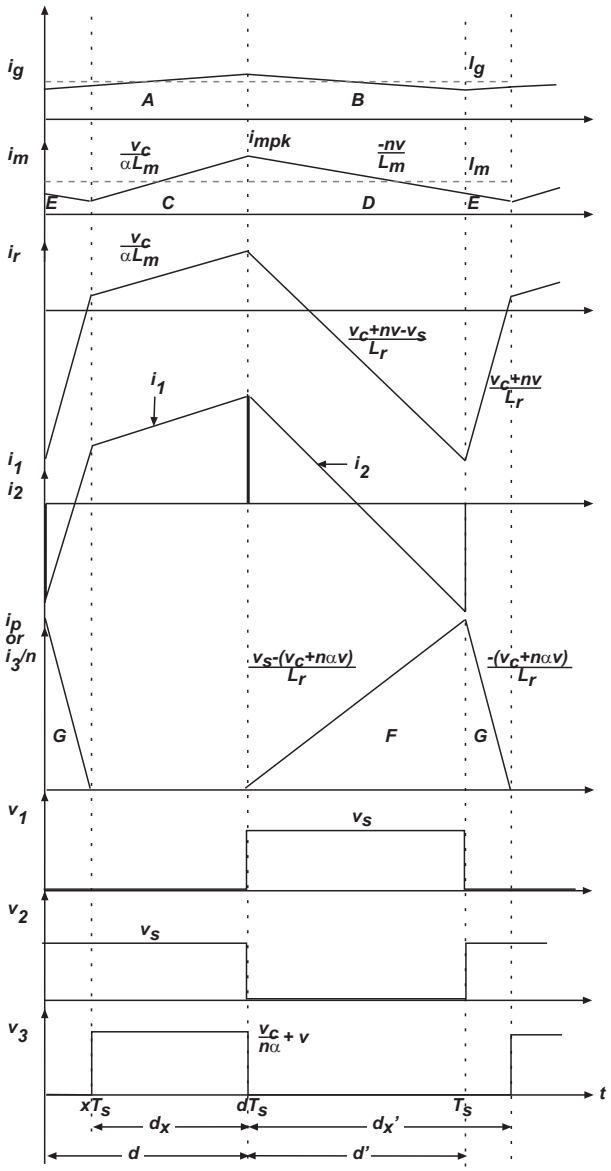

Fig. 16 Approximate waveforms for derivation of the model

$$\langle i_3 \rangle = n(F + G), \tag{22}$$

Areas *A* to *G* are found easily from the waveform geometry which is either a trapezoid or a triangle. For example, area *A* is equal to the base (dT_s) times the average height ($\langle i_g \rangle$).

$$A = d \langle i_g \rangle , \tag{23}$$

$$B = d' \langle i_g \rangle , \tag{24}$$

$$C = (d - x) \langle i_m \rangle , \tag{25}$$

D is the area under the magnetizing current waveform for time $d'T_s$ and is given by

$$D = \left(i_{mpk} + \left(i_{mpk} - \frac{n\langle v \rangle}{L_m} d'T_s \right) \right) \frac{d'}{2}, \quad (26)$$

where the peak current in the magnetizing inductance is

$$i_{mpk} = \langle i_m \rangle + \frac{n\langle v \rangle}{L_m} \cdot \frac{(d' + x)T_s}{2}, \quad (27)$$

$$\therefore D = d'\langle i_m \rangle + d' \frac{\beta x n \langle v \rangle}{R_e}, \quad (28)$$

finally we eliminate x from (28) by using (15), therefore,

$$D = d'\langle i_m \rangle + \frac{d'\langle i_3 \rangle \langle v \rangle \beta}{\left(\langle v_1 \rangle - d' \left(\langle v_c \rangle + nK \langle v \rangle \right) \right)} - \frac{d'^2 \beta n \langle v \rangle}{R_e}, \quad (29)$$

$$E = (d' + x)\langle i_m \rangle - D, \quad (30)$$

$$F = \frac{d'}{2} \left(\frac{\langle v_s \rangle - \left(\langle v_c \rangle + \alpha n \langle v \rangle \right)}{kL_m} \right) d'T_s, \quad (31)$$

$$\therefore F = \frac{d'}{R_e} \left[\langle v_1 \rangle - d' \left(\langle v_c \rangle + \alpha n \langle v \rangle \right) \right]_s, \quad (32)$$

$$G = \frac{\langle i_3 \rangle}{n} - F, \quad (33)$$

By adding (18) and (19) or adding (20) and (21) we get,

$$\langle i_1 \rangle + \langle i_2 \rangle + \frac{\langle i_3 \rangle}{n} = \langle i_g \rangle + \langle i_m \rangle, \quad (34)$$

Now, substituting the expressions *A*-*F* in (20) as required, we get the expression for $\langle i_1 \rangle$ as follows

$$\langle i_1 \rangle = \frac{d}{d'} \langle i_2 \rangle - \frac{\langle i_3 \rangle}{n} + \frac{d'\beta n \langle v \rangle}{R_e} - \frac{\beta \langle i_3 \rangle \langle v \rangle}{\left(\langle v_1 \rangle - d' \left(\langle v_c \rangle + \alpha n \langle v \rangle \right) \right)} + \frac{\left(\langle v_1 \rangle - d' \left(\langle v_c \rangle + \alpha n \langle v \rangle \right) \right)}{R_e}, \quad (35)$$

We can also choose to express $\langle i_2 \rangle$ in terms of the other quantities from (35).

From (11) and (12), we can see that

$$\langle v_2 \rangle = \frac{d}{d'} \langle v_1 \rangle, \quad (36)$$

This completes the derivation of the averaged switch model, which is given by (17), (35) and (36). This model can now be simulated with the help of a computer simulator.

APPENDIX B

PSpice Simulations

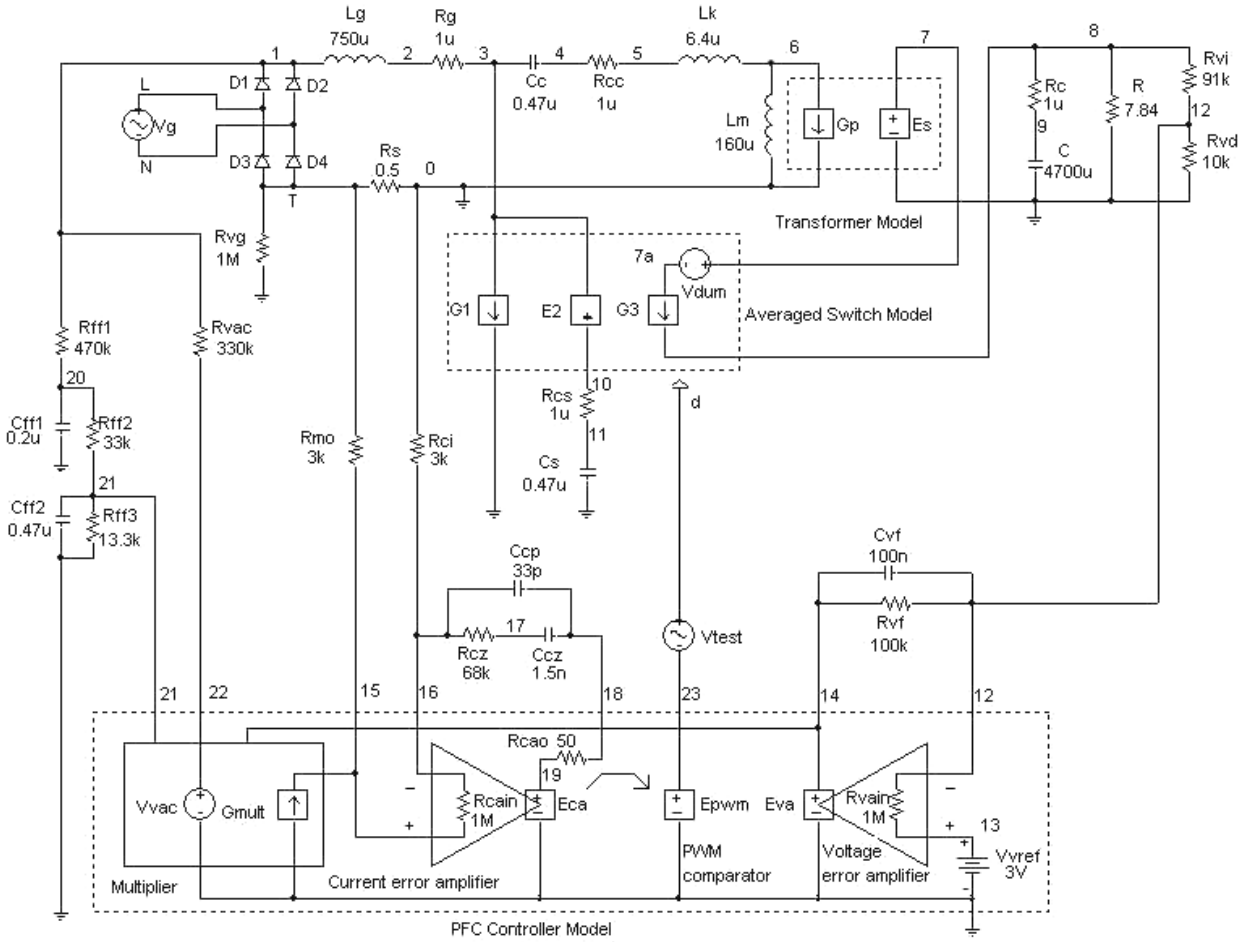

Fig. 17 PSpice schematic used for simulation of the rectifier prototype

PSpice Netlist

Active-clamped SEPIC rectifier simulation

.param Lg=0.75m Cc=0.47u Cs=0.47u C=4.7m beta=0.04 alpha={1+beta} Lm=160u Ts=5u n=4 Re={2*beta*Lm/Ts}
.nodeset v(21)=2.75; ***for dc analysis .nodeset and all initial conditions should be removed ; Result of the bias point calculation should be verified initially.***

*** Power stage**

Vg	L	N	SIN(0 163 400); ***for dc analysis this source should be Vg 1 T dc 115***
Rvg	N	0	1Meg
D1	L	1	D
D2	N	1	D
D3	T	L	D
D4	T	N	D
Rs	0	T	0.5
Lg	1	2	{Lg}
Rg	2	3	1u
Cc	3	4	{Cc}
Rcc	4	5	1u
Lr	5	6	{beta*Lm}

```
Lm      6       0       {Lm}
Rc      8       9       1u
C       9       0       {C}     IC=28
R       8       0       7.84
Rcs     10      11      1u
Cs      11      0       {Cs}
* Transformer model
Gp      0       6       value={i(Es)/n}
Es      7       0       value={v(6,0)/n}
** Controller
* Voltage error amplifier
Rvi     8       12      91k
Rvd     12      0       10k
Vvref   13      0       dc      3
Rvain   13      12      1Meg
Eva     14      0       value={LIMIT(V(13,12)*5000,0,10)}; LIMIT simulates the saturation of op-amp
Rvf     14      12      100k
Cvf     14      12      100n
* Voltage feedforward
Rff1    1       20      470k
Cff1    20      0       0.2u
Rff2    20      21      33k
Cff2    21      0       0.47u   IC=2.75
Rff3    21      0       13.3k
* Current command
Rvac    1       22      330k
Vvac    22      0       0.5
* Multiplier
Gmult   0       15      value={LIMIT(I(Vvac)*(V(14)-1)/V(21)/V(21),0,400u)},
* Current error amplifier and PWM comparator
Rmo     T       15      3k
Rci     0       16      3k
Rcain   15      16      1Meg
Rcao    19      18      50
Eca     19      0       value={LIMIT(V(15,16)*1e4,0,10)}
Epwm    23      0       value={LIMIT(V(18)/5.4,0.05,0.95)};   simulates saw tooth referenced PWM comparator
Rcz     16      17      68k
Ccz     17      18      1500p
Ccp     16      18      33p
Vtest   d       23      dc      0
************************************************
* Averaged switch model equations (36), (35) and (17) respectively are for E2, G1 and G3
E2      10      3       value=  {v(d)/(1-v(d))*v(3)}
G1      3       0       value=  {(v(d)/(1-v(d))*(-i(E2))-i(Vdum)/n
+(1-v(d))*beta*n*v(8)/Re-beta*v(8)*MAX(0,(n/Re*(v(3)-(1-v(d))*(v(3,4)+alpha*n*v(8)))
*(1-alpha*n*v(8,7)/(v(3,4)+alpha*n*v(8)))));                    has entire expression for G3 repeated for convergence
/(v(3)-(1-v(d))*(v(3,4)+alpha*n*v(8)))+(v(3)-(1-v(d))*(v(3,4)+alpha*n*v(8)))/Re)}
Vdum    7       7a      0
G3      7a      8       value=  {MAX(0,(n/Re*(v(3)-(1-v(d))*(v(3,4)+alpha*n*v(8)))
*(1-alpha*n*v(8,7)/(v(3,4)+alpha*n*v(8)))))};                   MAX simulates a unidirectional diode
************************************************
.model D D(vj=1V); diode model
* Analysis statements
.tran   5u      202.5m  200m    5u      UIC
.probe
.four 400 i(vg)
.op
.end
```