A Performance Model of Space-Division ATM Switches with Input and Output Queueing*

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Abstract

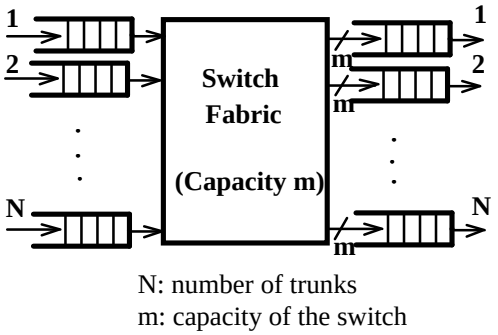
An analytic model for the performance evaluation of space-division Asynchronous Transfer Mode (ATM) switches is presented. This model assumes that the switch has a fixed capacity of m, *where* $1 \le m \le N$ (N *is the number of trunks*). *Other important parameters include arrival rate and buffer sizes. Numerical solutions for the maximum throughput, cell delay, and cell loss probability are given with simulation being utilized in order to validate the analytic model. For independent and identical Bernoulli arrivals, the study shows that the contention processes can be modeled as discrete* M/D/m *(FIFO or Random) queues, while input queues can be modeled by* Geom/G/1 *queues, and the output queues are* $G^{[x]}/D/1$ *queues. A closed-form approximation for cell delay when* $m>2$ *is given. The result shows that the performance of switches with a small capacity can approach that of output queueing. The model and result can be used for switch design analysis and higher layer performance models.*

1. Introduction

1.1 Analytic performance models: background

The performance analysis of ATM switches [1,2,3] has been attracting great attention in the recent years, and a number of models have been proposed and analyzed [4-15], with new models still appearing. The important model parameters of the current research on ATM switches include capacity, input/output buffering, buffer size, selection (arbitration) policy, synchronous or asynchronous operation mode, and various traffic patterns. This paper utilizes classical queueing theory to model the behavior of space-division ATM switches.

Figure 1. shows a general model of space-division ATM switches.



N: number of trunks
m: capacity of the switch

Figure 1. General model of an ATM switch

In a space-division ATM switch fabric, a plurality of paths is provided between the input and output ports. These paths operate concurrently so that many cells may be transmitted across the switch fabric at the same time. A space-division fabric can be further classified as single-path or multiple-path according to the number of paths between any given input and output pair (this number is often called the *capacity* of the switch). Space-division switches usually operate in synchronous mode, all cells in the input ports arriving at the switch fabric with their headers aligned to simplify the design. In a time-division based switch fabric, cells flow across a single communication highway shared by all input and output ports. This research is aimed at space-division models.

The primary performance criteria of an ATM switch are throughput, cell delay, and cell loss probability. Definitions of each are as follows:
Throughput of an ATM switch is the percentage of total cells leaving the output to the total time slots. Cell delay is the time from a cell arrival to the input port, to the cell departure from the output port. Cell loss probability is the probability that a cell will be lost in the switch fabric due to the lossy contention resolution mechanism.

* The work was done when G. Zhang was at University of Kansas.

The article by Hluchyj, *et al*. [5] contains an excellent review of queueing in ATM switches. In general, the typical models of ATM switches are categorized into three broad classes, namely, output queueing, input queueing, and input and output queueing. This research explores a model of input and output queueing.

1.2 Analytic performance models: our research

Based on research presented, our study was designed to investigate a general analytic model of an ATM switch. The fixed capacity of the switch and the buffer sizes are important parameters that distinguish this research from prior research. The important performance criteria include cell delay, throughput and cell loss probability.

Our model is different from the input and output queueing model presented in [6] in that backpressure due to output buffer being full is not considered (contention policy), and cell loss probability is calculated. In [6], the capacity of the switch is not fixed and backpressure is applied when the output buffers are full (no cell loss is possible). It is our belief that our model reflects the reality of many ATM designs and therefore is of practical significance.

2. A model for input and output queueing

For this model, the following assumptions are made:

(1) Cell arrivals on the N inputs are independent and identical Bernoulli processes. In any given time slot, the probability that a cell will arrive on a particular input is p, where $0 < p \le 1$.

(2) Each cell has equal probability $1/N$ of being addressed to any given output, and successive cells are independent.

(3) The switch capacity is m, where $1 \le m \le N$. That is, if there are k cells at the heads of input queues and destined for the same output port, only m cells can be routed to the output queue at one time if $k>m$. The others wait for next chance. The selection policy can be random or FIFO.

(4) There are B buffers at each output, where B can be infinity. There are infinite buffers at each input. It is reasonable to assume that $B \ge m$.

Notice that assumptions (1) and (2) are the same as the previous model assumptions. Assumption (3) differentiates the selection (arbitration) policy between random and FIFO. References [4,6,7] discuss the differences between these two policies. Their study and our simulation result [16] show that the difference between these two policies is negligible and we will focus our analysis on FIFO. The input queueing is a special case of our model with $m = 1$, and the output queueing, $m = N$.

The analysis is divided into two separate cases. Case I is when both N and B are large (the limiting case). Case II is when N is large and output buffer size B is finite (limited). In both of these situations, the contention process, the output queue and the various performance criteria, which include the cell delay, the throughput, and possible cell loss are considered.

2.1 Case I: limiting analysis (FIFO with *N* and *B* infinite)

In this section, we present an approximate model for large N and large output buffer size B. The analysis is divided into three sections: the contention process; the output queue; and the performance criteria.

Contention process. During each time slot, cells at the heads of input queues and destined for the same output contend to be routed to the output. These contending cells form a logical queue. There is one such contention queue for each output and in steady-state each is symmetric and statistically identical.

For a tagged output contention queue, define:

A_i: the number of cell arrivals to the heads of input queues and destined for the tagged output during the ith time slot;

C_i: the number of cells in the tagged queue at the end of the ith time slot.

We have

$$C_i = \max(C_{i-1} - m, 0) + A_i$$

The limiting distribution of A_i is Poisson [4,6]:

$$a_k \overset{\Delta}{=} \Pr[A_i = k] = \frac{p^k e^{-p}}{k!}, \quad k = 0,1,2,\cdots \qquad (1)$$

Using this result, the contention process can be modeled as an *M/D/m* queue. The *M/D/m* queue is a Markov chain with its state represented by the value of C_i. The transition probability from state j to state l in adjacent slots is given by a_{l-j+m} for $j \ge m$, or a_l for $j < m$. Denote $\mathbf{Q}$ the state transition matrix of the Markov chain, which is

$$\mathbf{Q} = \begin{array}{c} 0 \\ \vdots \\ m-1 \\ m \\ m+1 \\ m+2 \\ \vdots \end{array} \begin{pmatrix} a_0 & a_1 & a_2 & a_3 & \cdots \\ \vdots & \vdots & \vdots & \vdots & \ddots \\ a_0 & a_1 & a_2 & a_3 & \cdots \\ a_0 & a_1 & a_2 & a_3 & \cdots \\ 0 & a_0 & a_1 & a_2 & \cdots \\ 0 & 0 & a_0 & a_1 & \cdots \\ \vdots & \vdots & \vdots & \vdots & \ddots \end{pmatrix}$$

Let the steady-state probability $p_j \overset{\Delta}{=} \lim_{i\to\infty} \Pr[C_i = j]$, and $\mathbf{p} = (p_0, p_1, p_2, \ldots)$. We have the balance equations

$$\mathbf{p}(\mathbf{I}-\mathbf{Q})=\mathbf{0}, \text{ and } \mathbf{p1}=1 \quad (2)$$

where **I** is the identity matrix and **1** is the column vector with all elements equal to 1. For the system under steady state, there is a unique solution for this equation system.

Let $\mathbf{n} = (0,1,2,3,...,i,...)$ and $\mathbf{n}_2 = (0,1,4,9,...,i^2,...)$, the first and second moments of number in the contention process are

$$\overline{C} = \mathbf{p}\cdot\mathbf{n}^{\mathrm{T}} \quad (3)$$

and

$$\overline{C^2} = \mathbf{p}\cdot\mathbf{n}_2^{\mathrm{T}}. \quad (4)$$

The first moment of time in the contention process is given by Little's result as

$$\overline{S} = \frac{\overline{C}}{p} \quad (5)$$

and the second moment of time is given by the generalization of Little's result [17] as

$$\overline{S^2} = \frac{(\overline{C^2}-\overline{C})}{p^2}. \quad (6)$$

Output queue. For the output queue, the arrival is the departure from the contention process, which is modeled by a discrete-time *M*/*D*/*m* queue with average departure rate *p*. Therefore, the number of cell arrivals E_i to the output queue has random batch size from 0 to *m* with probability distribution given by

$$d_k \overset{\Delta}{=} \Pr[E_i = k] = \begin{cases} p_k & k = 0,1,\ldots,m-1; \\ \sum_{j=m}^{\infty} p_j & k = m; \\ 0 & k > m; \end{cases} \quad (7)$$

Denote V_i the number of cells in the output queue at the end of the *i*th time slot. We have

$$V_i = \max(V_{i-1}-1,0)+E_i \ . \quad (8)$$

Therefore, the output queue is a discrete-time $G^{[x]}/D/1$ queue. It can be modeled by a discrete-time Markov chain with its state represented by the value of V_i. The transition probability from state *j* to state *l* in adjacent slots is given by d_{l-j+1} for $j \geq 1$, or d_l for $j=0$. Denote **R** the state transition matrix of the Markov chain, which is

$$\mathbf{R} = \begin{matrix} 0 \\ 1 \\ 2 \\ 3 \\ \vdots \end{matrix} \begin{pmatrix} d_0 & d_1 & d_2 & \cdots & d_m & 0 & \cdots \\ d_0 & d_1 & d_2 & \cdots & d_m & 0 & \cdots \\ 0 & d_0 & d_1 & \cdots & d_{m-1} & d_m & \cdots \\ 0 & 0 & d_0 & \cdots & d_{m-2} & d_{m-1} & \cdots \\ \vdots & \vdots & \vdots & \cdots & \vdots & \vdots & \ddots \end{pmatrix}. \quad (9)$$

Let the steady-state probability $v_j \overset{\Delta}{=} \lim_{i\to\infty} \Pr[V_i = j]$, and $\mathbf{v} = (v_0, v_1, v_2, \ldots)$. We have the balance equations

$$\mathbf{v}(\mathbf{I}-\mathbf{R}) = \mathbf{0}, \text{ and } \mathbf{v1} = 1 \quad (10)$$

For the system under steady state, there is a unique solution for this equation system as follows.

$$\begin{aligned} v_0 &= 1-p; \\ v_1 &= \frac{1-d_0}{d_0} v_0; \\ v_i &= \frac{1-d_1}{d_0} v_{i-1} - \frac{d_{i-1}}{d_0} v_0 - \sum_{j=2}^{i-1} \frac{d_j}{d_0} v_{i-j}, \ \text{For } i \geq 2 \end{aligned} \quad (11)$$

The average number in the output queue is given by $\overline{V} = \mathbf{v}\mathbf{n}^T$. By Little's result, the mean time in the output queue, denoted by $\overline{D}_{out}$, is

$$\overline{D}_{out} = \frac{\overline{V}}{p}. \quad (12)$$

Performance criteria. For a tagged cell, the total delay in the system contains three components: waiting in the input queue until moving to the head of the queue; time in the contention process at the head of the queue; and time in the output queue. We denote these three delay components by D_{in}, D_{cp}, and D_{out}, respectively.

For the input queue, the arrival process is Bernoulli, that is, the interarrival time is geometrically distributed. The service time is the time in the contention process, which has general distribution with the first and second moments of time obtained as equations (5) and (6) above. Therefore the input queue is a discrete-time *Geom*/*G*/1 queue. The average waiting time is given by

$$\overline{D}_{in} = \frac{p(\overline{S^2}-\overline{S})}{2(1-p\overline{S})} \quad (13)$$

And we have

$$\overline{D}_{cp} = \overline{S}.$$

The average time in the output queue is given by (12).

The average total delay becomes

$$\overline{D} = \overline{D}_{in} + \overline{D}_{cp} + \overline{D}_{out} = \frac{p(\overline{S^2}-\overline{S})}{2(1-p\overline{S})} + \overline{S} + \frac{\overline{V}}{p}. \quad (14)$$

In order to obtain the maximum throughput, steady state is assumed. It is required that both the input queue and the output queue be in steady state. For the input queue, from (13), the condition is

$$1-p\overline{S} > 0. \quad (15)$$

Since $\overline{S}$ is a function of *p*, which cannot be expressed in closed form, we need to use numerical method to get the value. For the output queue, which is $G^{[x]}/D/1$, the requirement is $p \leq 1$, because *p* is the mean arrival rate. This condition is subsumed by the assumption and (15). Therefore the maximum throughput is determined by solving (15) for the upper bound of *p*.

2.2 Case II: analysis for large *N* and finite *B*

In this section, we present an approximate model for

large N and limited output buffer B. In practice, N and B are always limited.

Assume that there are only a finite number of B buffers available at each output port. The output queue becomes discrete-time $G^{[x]}/D/1/B$ queue. The cells will be lost if not enough output buffers are available to accommodate all cells.

Contention process. When N is large, the arrival to the contention queue can be approximated by the same Poisson arrival distribution as in (1) [6]. The contention process is modeled by an *M/D/m/N* queue. To calculate the steady-state probabilities, we model this *M/D/m/N* queue by a finite state Markov chain. The state transition matrix **Q** of this Markov chain becomes

$$\mathbf{Q} = \begin{array}{c} 0 \\ \vdots \\ m-1 \\ m \\ m+1 \\ m+2 \\ \vdots \\ N \end{array} \begin{pmatrix} a_0 & a_1 & a_2 & a_3 & \cdots & a_{N-1} & 1-\sum_{i=0}^{N-1} a_i \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ a_0 & a_1 & a_2 & a_3 & \cdots & a_{N-1} & 1-\sum_{i=0}^{N-1} a_i \\ a_0 & a_1 & a_2 & a_3 & \cdots & a_{N-1} & 1-\sum_{i=0}^{N-1} a_i \\ 0 & a_0 & a_1 & a_2 & \cdots & a_{N-2} & 1-\sum_{i=0}^{N-2} a_i \\ 0 & 0 & a_0 & a_1 & \cdots & a_{N-3} & 1-\sum_{i=0}^{N-3} a_i \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & 0 & \cdots & a_{m-1} & 1-\sum_{i=0}^{m-1} a_i \end{pmatrix}_{(N+1)\times(N+1)}$$

Let the steady-state probability vector be $\mathbf{p} = (p_0, p_1, p_2, ..., p_N)$. The balance equations are

$$\mathbf{p}(\mathbf{I}-\mathbf{Q}) = \mathbf{0}, \quad \text{and} \quad \mathbf{p1} = 1 \tag{16}$$

From this equation system, **p** can be solved numerically. The first and second moments of the time in the contention process are

$$\overline{S} = \frac{1}{p}\sum_{i=1}^{N} i \cdot p_i \tag{17}$$

and

$$\overline{S^2} = \frac{1}{p^2}\sum_{i=1}^{N} (i^2 - i) \cdot p_i \tag{18}$$

Output queue. The number of cell arrivals E_i to the output queue has random batch size from 0 to m with probability distribution given by

$$d_k = \Pr[E_i = k] = \begin{cases} p_k & k = 0,1,...,m-1; \\ \sum_{j=m}^{N} p_j & k = m; \\ 0 & k > m; \end{cases} \tag{19}$$

The output queue is a discrete-time $G^{[x]}/D/1/B$ queue. The state transition matrix **R** of this finite state discrete-time Markov chain becomes

$$\mathbf{R} = \begin{array}{c} 0 \\ 1 \\ 2 \\ 3 \\ \vdots \\ B \end{array} \begin{pmatrix} d_0 & d_1 & d_2 & \cdots & d_m & 0 & \cdots & 0 \\ d_0 & d_1 & d_2 & \cdots & d_m & 0 & \cdots & 0 \\ 0 & d_0 & d_1 & \cdots & d_{m-1} & d_m & \cdots & 0 \\ 0 & 0 & d_0 & \cdots & d_{m-2} & d_{m-1} & \cdots & 1-\sum d_i \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & 0 & 0 & \cdots & 1-d_0 \end{pmatrix}_{(B+1)\times(B+1)}$$

Let the steady-state probability vector be $\mathbf{v} = (v_0, v_1, v_2, ..., v_B)$. The balance equations are

$$\mathbf{v}(\mathbf{I}-\mathbf{R}) = \mathbf{0}, \quad \text{and} \quad \mathbf{v1} = 1 \tag{20}$$

We can get the numerical solution for **v**. The mean number of cells in the output queue is

$$\overline{V} = \sum_{i=1}^{B} i \cdot v_i . \tag{21}$$

Performance criteria. The probability of the output queue being idle is v_0. Therefore the effective throughput from the output queue is

$$T = 1 - v_0. \tag{22}$$

When the output buffers are full or free buffers are not enough, all or part of the new cell arrivals to the output queue will be lost. The cell loss probability is therefore equal to

$$\Pr[\textit{cell loss}] = 1 - \frac{T}{p} = 1 - \frac{1-v_0}{p}. \tag{23}$$

By Little's result, the average waiting time in the output is

$$\overline{D}_{out} = \frac{\overline{V}}{T} \tag{24}$$

The average cell delay is given by

$$\overline{D} = \overline{D}_{in} + \overline{D}_{cp} + \overline{D}_{out} = \frac{p(\overline{S^2} - \overline{S})}{2(1-p\overline{S})} + \overline{S} + \frac{\overline{V}}{1-v_0}. \tag{25}$$

where $\overline{S}$, $\overline{S^2}$, and $\overline{V}$ are given by (17), (18) and (21), v_0 is the probability of the output queue being idle obtained from (20).

2.3 Simple numerical method for limited case

We need to solve equation systems (16) and (20) to get the values for throughput, cell loss probability, and cell delay.

Solution for the contention process. For the balance equations of the contention process (16), one simple way to get the solution is from the relationship

$$\mathbf{p}_{i+1} = \mathbf{p}_i \cdot \mathbf{Q}$$
$$\mathbf{p} = \lim_{i \to \infty} \mathbf{p}_i \tag{26}$$

if an appropriate initial vector $\mathbf{p}_0$ is given, for instance,

$$\mathbf{p_0} = (\frac{1}{N+1}, \frac{1}{N+1}, \ldots, \frac{1}{N+1})_{N+1}.$$

Because $\mathbf{p}_0\mathbf{1} = 1$, by induction,

$$\mathbf{p}_{i+1}\mathbf{1} = \mathbf{p}_i\mathbf{Q}\mathbf{1} = \mathbf{p}_i\mathbf{1} = 1.$$

The simple iteration of the first equation in (26) will converge rapidly and result in the accurate solution for (16).

Solution for the output queue. We can write out the recurrence relation of the solution to the balance equation of the output queue (20) as follows.

$$p_1 = \frac{1}{d_0}(1-d_0)\,p_0,$$
$$p_i = \frac{1}{d_0}((1-d_1)\,p_{i-1} - d_{i-1}p_0 - \sum_{j=1}^{i-2} d_{i-j}\,p_j), \quad \text{for } 2 \le i \le m;$$
$$p_i = \frac{1}{d_0}((1-d_1)\,p_{i-1} - \sum_{j=i-m+1}^{i-2} d_{i-j}\,p_j), \quad \text{for } m < i \le B; \tag{27}$$

where p_0 is determined by

$$\sum_{i=0}^{B} p_i = 1.$$

From (27), we see that $p_i = c_i\, p_0$ for some constants c_i. We can easily get c_i by setting $p_0 = 1$ from (27) and

$$p_0 = \left(1 + \sum_{i=1}^{B} c_i\right)^{-1}. \tag{28}$$

We can also use the same method for (16) above to get numerical results for (20).

3. Results

Simulation models [16] were used to validate the analytic model. The result shows that the analytic model is very accurate under its assumptions. In the following, some of the results are listed. They are divided into three sections: throughtput, cell delay, and cell loss probability.

3.1 Throughput

The maximum throughput for various values of *m* from both numerical analysis and simulation is listed in Table 1.

Table 1. Capacity versus max. throughput (for N=20)

Capacity (m)	Throughput (Numerical result)	Throughput (Simulation)
1	0.585781	0.5959
2	0.884529	0.8961
3	0.975494	0.9784
4	0.995583	0.9932
5	0.999306	(not available)
6	0.999901	(not available)
7	0.999985	(not available)

For example, consider trunks with 622.08 Mb/s (STM-3) rate. In order to support a 90% throughput, i.e. a rate of 622.08 * 90% = 560 Mb/s, the switch capacity *m* must be greater than 2. Similarly, if we consider the switch cycle for trunks with 155.52 Mb/s (STM-1) rate, and we want to support 90% throughput (140 Mb/s) with speed-up switch fabrics, then the switch cycle needs to be 1/3 of the time slot (m>2), i.e., about 0.91 msec.

For another example, if a space-division switch is to support 600 Mb/s rate on a 622.08 Mb/s rate trunk (throughput=0.9645), the switch capacity should be at least 3.

3.2 Cell delay

Delay time in the input queue (including contention time), in the output queue, and total cell delay from numerical analysis for different *m* and *p* is plotted in figures 2, 3, and 4.

When *m* becomes large, the switch performance will approach that of output buffering. The mean cell delay in the system for *m*>2 can be approximated by delay in an *M/D*/1 system with arrival rate *p* and constant service time (one slot per cell), i.e.,

$$\overline{D} \approx 1 + \frac{p}{2(1-p)}$$

The comparison of this approximation with numerical result is listed in Table 2 and sketched in Figure 5.

Since one time slot is 53 bytes, the time slot for 155.52 Mb/s rate is about 2.73 ms, and 0.682 ms for 622.08 Mb/s rate. If switches in the network are under normal load (about 80% of maximum throughput), then the delay introduced by a switch is only several time slots long, and comparable with cell propagation delay in several kilometers distance.

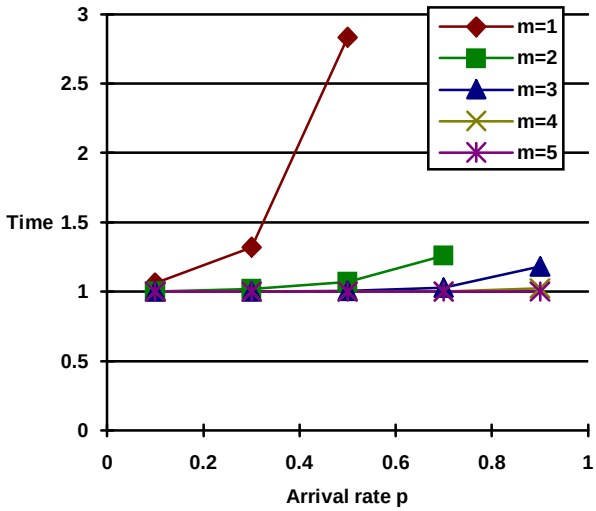


Figure 2. Time slots in input queues(including contention time)

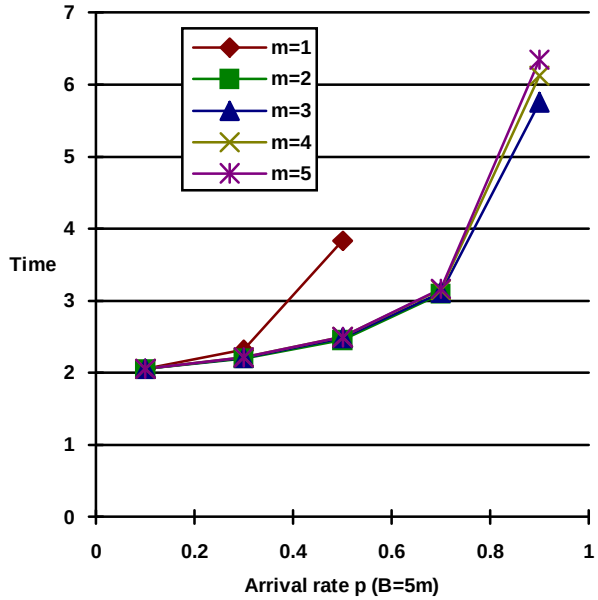


Figure 4. Total cell delay (time slots)

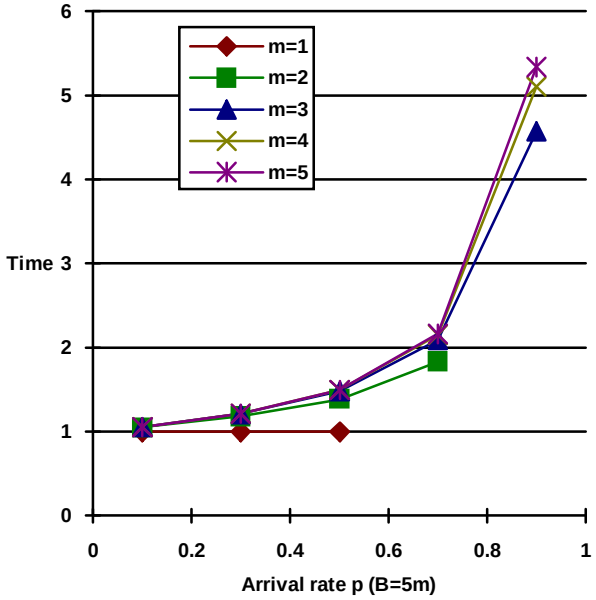


Figure 3. Time slots in output queues

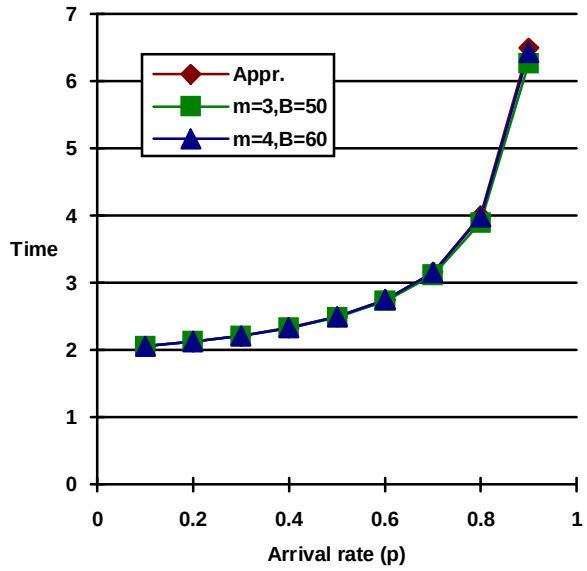


Figure 5. Cell delay from approximation and numerical analysis

3.3 Cell loss probability

Cell loss probability for various values of *m* and *B* from numerical analysis is listed in Table 3.

If the cell loss probability needs to achieve 10^{-7} under the load of maximum throughput of 80%, the output buffers should be at least 6*m*, where *m* is the capacity of the switch. And the buffer size needs to be much larger for peak rate in bursty traffic to prevent cell loss.

4. Discussion and future research

Our model is a straight forward model of the operation of switches. The one exception is the arrival process, which is confined to Bernoulli. The simulation result shows that the analytic model is an accurate model of switches under the assumptions.

Because the exact closed-form solution are very

difficult to obtain, an approximate formula for cell delay when $m>2$ is given and can be applied easily.

The applicability of the model depends on the validity of the assumptions of arrival process and random destination of cells. In a networked environment, the arrival to a trunk of a switch will be a merger of a large number of connections from many different sources, to many different destinations. By virtue of Palm-Khintchine's theorem, this merged process will approach a Poisson process in continuous situation, while in discrete time, we conjecture that Bernoulli is the limiting process. The result from [10] is additional evidence that the assumptions are appropriate in many cases.

The model can be easily extended to non-uniform traffic. And models with other traffic patterns will be explored further. In particular, we will be using algebraic queueing theory and simulation models to better model the traffic patterns and analyze the statistical and dynamic behavior of switches.

Further studies will investigate more performance issues within the higher layers of ATM and B-ISDN systems.

Table 2. Mean time from discrete M/D/1 *queue vs. cell delay from numerical result for m=2,3,4*

Rate(p)	Appr. Time	m=2, B=40	m=3,B=50	m=4,B=60
0.1	2.055556	2.0539	2.0555	2.0556
0.2	2.125000	2.1184	2.1243	2.1250
0.3	2.214286	2.1992	2.2119	2.2141
0.4	2.333333	2.3058	2.3272	2.3326
0.5	2.500000	2.4556	2.4869	2.4980
0.6	2.750000	2.6856	2.7242	2.7452
0.7	3.166667	3.0939	3.1170	3.1559
0.8	4.000000	4.0942	3.8997	3.9748
0.9	6.500000	(Not Applicable)	6.2602	6.4261

Table 3. Cell loss probability with various buffer sizes(B)

capacity (m)	arrival rate (p)	buffer size B=2m	buffer size B=4m	buffer size B=6m
1	all	0.0000000000	0.0000000000	0.0000000000
2	0.1	0.0000000065	0.0000000000	0.0000000000
2	0.3	0.0000164004	0.0000000001	0.0000000000
2	0.5	0.0006864941	0.0000004706	0.0000000003
2	0.7	0.0080605249	0.0001461056	0.0000026963
3	0.1	0.0000000001	0.0000000000	0.0000000000
3	0.3	0.0000015654	0.0000000000	0.0000000000
3	0.5	0.0001809394	0.0000000415	0.0000000000
3	0.7	0.0041738772	0.0004350973	0.0000005056
3	0.9	0.0348799413	0.0070481351	0.0016797473
4	0.1	0.0000000000	0.0000000000	0.0000000000
4	0.3	0.0000000500	0.0000000000	0.0000000000
4	0.5	0.0000226298	0.0000000007	0.0000000000
4	0.7	0.0013785400	0.0000053372	0.0000000207
4	0.9	0.0230213348	0.0035892405	0.0006375607
5	0.1	0.0000000000	0.0000000000	0.0000000000
5	0.3	0.0000000011	0.0000000000	0.0000000000
5	0.5	0.0000021516	0.0000000000	0.0000000000
5	0.7	0.0003875106	0.0000004333	0.0000000005
5	0.9	0.0146580192	0.0016369826	0.0002013317

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