

## Introduction

SDRAM is commonly used in cost-sensitive applications requiring large amounts of memory. Though SDRAM is inexpensive, the implementation of refresh operations, open row management, and various delays and command sequences requires logic. The Nios SDRAM Controller with an Avalon interface, transparently handles SDRAM initialization, refresh, and all other SDRAM requirements, and appears to software as a simple linear memory interface (flat address space) with a wait signal. The SDRAM Controller supports standard SDRAM as described in PC100. With the SDRAM Controller, users can access SDRAM subsystems with data widths of 16-bit or 32-bit, various memory sizes, and multiple chip selects.

## PTF Assignments

A particular instantiation of the SDRAM Controller is generated according to parameters configured in the system PTF file. The parameters take into account:

- system clock frequency
- SDRAM timing assignments
- size of SDRAM row and column addresses
- number of SDRAM chipselect signals
- choice of options governing the performance vs. complexity trade-off

Designers use the SDRAM Controller configuration wizard in SOPC Builder to assign timing parameters for a specific SDRAM device. The timing parameters (including the requested system frequency) are used to determine all of the controller's timing values (in integer multiples of system clock cycles). Regardless of the input value, the timing will be based on the system clock frequency and timing will be the number of clock ticks that provide a value greater than or equal to the input value.

The SDRAM Controller is built for a particular application according to the assignments in the system PTF file. Generating a controller for a new SDRAM configuration requires configuring the SDRAM Controller's size and timing. This can be done in one of two ways:

1. Change the settings in the SDRAM Controller's SOPC Builder configuration wizard.
2. Edit the SDRAM Controller PTF file's size and timing assignments.



See the *SOPC Builder Data Sheet* for more information about the SOPC Builder configuration wizards and see the *SOPC Builder PTF File Reference Manual* for PTF file assignment details.

Tables 1 through Table 4 on page 3 list the SDRAM Controller PTF parameters. All of these parameters are located in the system PTF's MODULE/WIZARD\_SCRIPT\_ARGUMENTS section.

Parameter	Type	Allowed Values	Default	Units	Description
sdr_data_width	Integer	8, 16, 32	32	bits	SDRAM data bus width.
sdr_addr_width	Integer	(*)	11	bits	Number of SDRAM address pins. Normally the same as sdr_row_width.
sdr_bank_width	Integer	2	2	bits	Number of SDRAM bank address pins. Must be 2 (4 banks).
sdr_num_chipselects	Integer	1, 2, 4	1	bits	Number of independent chip selects in the SDRAM system.

Parameter	Type	Allowed Values	Default	Units	Description
sdr_row_width	Integer	$\geq 11$	11	bits	Number of row address bits. This value depends on SDRAM geometry. For example, an SDRAM organized as 4096 rows by 512 columns has sdr_row_width = 12.
sdr_col_width	Integer	$\geq 8$ and $< \text{sdr\_row\_width}$	8	bits	Number of column address bits. For example, the SDRAM organized as 4096 rows by 512 columns has sdr_col_width = 9.

Parameter	Type	Allowed Values	Default	Units	Description
refresh_period	Floating Point	(*)	15.625	$\mu\text{s}$	One refresh command is executed each refresh_period. A typical SDRAM requires 4096 refresh commands every 64ms, which can be met by issuing one refresh command every $64\text{ms} / 4096 = 15.625\mu\text{s}$ .
powerup_delay	Floating Point	(*)	100	$\mu\text{s}$	The delay from stable clock and power to SDRAM initialization.

**Table 3. Timing (Part 2 of 2)**

Parameter	Type	Allowed Values	Default	Units	Description
cas_latency	Integer	1, 2	1	clock cycles	Latency in clocks from a READ command to data out. Typical SDRAM chips support CAS latency of 2 or 3; rare examples also support CAS latency = 1. For best performance, use the lowest CAS latency possible, but beware of increased t <sub>AC</sub> at lower CAS latencies.
t <sub>rfc</sub>	Floating Point	(*)	70	ns	Auto-refresh period.
t <sub>rp</sub>	Floating Point	(*)	20	ns	PRECHARGE command period.
t <sub>mrd</sub>	Floating Point	(*)	2	clocks	LOAD MODE REGISTER command to ACTIVE or REFRESH command. JEDEC and PC100 specify 3 clocks; other parts accept 2 clocks.
t <sub>rcd</sub>	Floating point	(*)	20	ns	ACTIVE to READ or WRITE delay.
t <sub>ac</sub>	Floating point	(*)	17	ns	Access time from clock edge. This value may depend on CAS latency.
t <sub>wr_precharge</sub>	Floating point	(*)	14	ns	Write recovery if explicit PRECHARGE commands are issued (highperf = 1).
init_refresh_commands	Integer	(*)	2		The number of refresh commands required during initialization. The SDRAM controller logic is minimized by smaller values of this parameter.

**Table 4. Advanced**

Parameter	Type	Allowed Values	Default	Units	Description
init_nop_delay	Floating point	(*)	0	μs	The required delay after the first NOP command during initialization. Other parts require no additional delay.
enable_ifetch	Boolean	0	0	–	Reserved for future use.
shared_data	Boolean	0	0	–	Requires tri-state bus bridge.

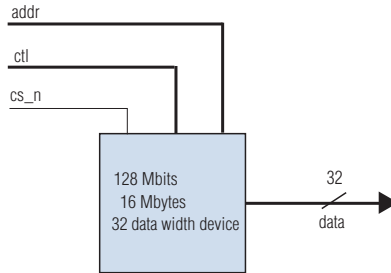
(\*) The correct values depend upon the information provided in the SDRAM manufacturer's data sheet.

## Examples

The following examples show how to connect the SDRAM controller outputs to an SDRAM chip or chips. The bus labeled `ctl` is an aggregate of the signals `cas_n`, `ras_n`, `cke` and `we_n`.

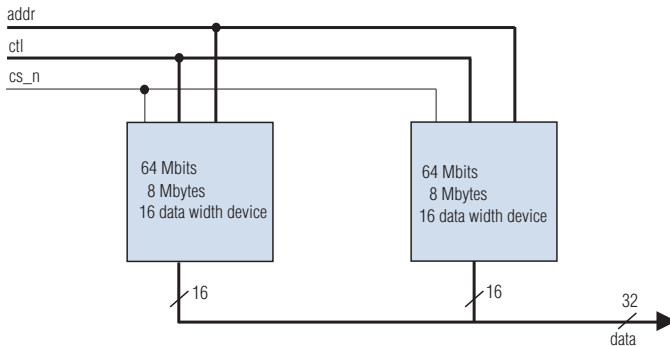
**Figure 1** shows a single 128 Mbit SDRAM chip with 32-bit data. Address, data and control signals are wired directly from the controller to the chip. The result is a 128Mbit (16Mbyte) memory space.

**Figure 1. Single 128 Mbit SDRAM Chip with 32-Bit data**



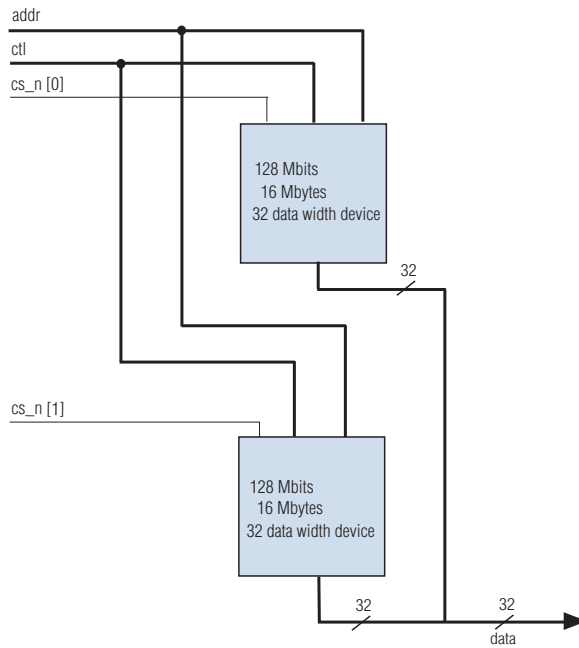
**Figure 2** shows two 64Mbit SDRAM chips, each with 16-bit data. Address and control signals wire in parallel to both chips. Note that chipselect (`cs_n`) is shared by the chips. Each chip provides half of the 32-bit data bus. The result is a logical 128Mbit (16Mbyte) 32-bit data memory.

**Figure 2. Two 64Mbit SDRAM Chips each with 16-Bit Data**



**Figure 3** shows two 128Mbit SDRAM chips, each with 32-bit data. Control, address and data signals wire in parallel to the two chips. The chipselect bus (`cs_n[1:0]`) determines which chip is selected. The result is a logical 256Mbit 32-bit wide memory.

**Figure 3. Two 128Mbit SDRAM Chips each with 32-Bit Data**





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