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ENCODING SCHEME FOR CROSSTALK MINIMIZATION

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ABSTRACT

Crosstalk in on-chip buses ends up in serious issues relating delay and power dissipation. Many encoding techniques were proposed avoid crosstalk step-down. Fibonacci based coding reduces the amount of transitions within the code words and therefore moves itself closed to an entire resolution for crosstalk step-down. The crosstalk impact may be a consequence of coupling and switching activities that's encountered once there is a transition as compared to previous state of wire and once there are transitions in adjacent wires. There are many strategies for the reduction of power dissipation, crosstalk and delay. This paper proposes encoding theme to realize the crosstalk. This coding technique is enforced mistreatment VHDL. This proposed algorithmic program is cut back the crosstalk and delay.

Keywords: crosstalk, switching activities, power dissipation, delay.

1. INTRODUCTION

In the deep sub micrometer technology, resistance, length, capacitance are increasing considerably, that contribute to massive on chip interconnect propagation delay [2]. Knowledge transmitted over interconnect confirm the propagation delay and also the delay is extremely important once adjacent wires are transitioning in opposite directions as compared to transitioning with in the same direction. The energy dissipation is directly proportional to the amount of transitions (1 to 0(or) 0 to 1). On the wires of the bus the cross-talk is directly proportional to the number of adjacent transitions (1to 0 (or) 0 to 1) transitions on adjacent wires at the identical time) ((1to 0 or 0 to 1) within the bus [12]. However, for on-chip buses, the main issue in terms of power consumption is concerning the inter-wire coupled capacitance, minimizing this is often key for reducing power consumption. During this paper, we tend to propose an adaptive encoding technique that targets the matter of each bus step-down and interference reduction [5]. By relating Fibonacci number system to crosstalk-free codes, we tend to crosstalk-free encoding technique and provided are cursive procedure to get such codes. Fibonacci number system in such the simplest way that 01 or 10 on two adjacent bits are prohibited. In impermissible pattern free interference turning away committal to writing [1], data are encoded mistreatment Fibonacci number system in such a way that 010 and 101 patterns are prohibited. [1]. in this paper, we tend to an adaptive encoding method that targets the problem of both bus transition minimization and crosstalk reduction. Conjointly minimize the ability and space.

2 FIBONACCI NUMBER SYSTEMS

A number system S=(U,C) is outlined by a strictly increasing sequence of positive integers $U=(U_n)\geq 0$ and a finite set of positive integers. Parts of sets U and C are referred to as the premise parts and digits of the amount system, severally. [1]. The binary number representation system is outlined as $S=((2^n)_{n\geq 0})\{0,1\}$. Fibonacci number system of order s, s≥2 is outlined as $S=(F_s,\{0,1\})$ wherever $F_s=(f_n)\geq 0$ such that

$F_i=2^i$

$F_i=f_{i-1}+...+f_{i-s}$ for i≥0

It has been shown that Fibonacci number system of order s.s≥2 is complete [13]. Each whole number could have multiple illustration in $S=(F_s,\{0,1\})$. Note that an whole number could have multiple representations in Fibonacci number system of orders,s≥2, To overcome the ambiguity in representing integers in Fibonacci number system of order s,s≥2 a normal-form [13] is outlined, whereever in each whole number features a distinctive illustration that does not contain consecutive bits equal to 1.

3. ON-CHIP CROSSTALK AVOIDANCE

Capacitive interference has become a major determinant of the full power consumption and delay of on-chip busses. Figure-1 illustrates a simplified on-chip bus model with crosstalk. In the Figure, CL denotes the load capacitance, which has the receiver gate capacitance and conjointly the parasitic wire-to-substrate parasitic capacitance. CI is that the inter-wire coupling capacitance between adjacent signal lines of the bus. In observe this bus structure is usually modeled as a distributed RC network, which has the nonzero resistance of the wire as well It's been shown that for DSM processes, CI is way larger than CL[8, 13]. Based on the energy consumption and delay models given within the bus energy consumption are often derived as a perform of the full crosstalk over the whole bus. The worst case delay, that determines the most speed of the bus, is proscribed by the most crosstalk that any wire within the bus incurs. It's

been shown that reducing the crosstalk boosts the bus performance considerably totally. Different approaches are proposed for crosstalk reduction within the context of bus interconnects. Some schemes specialise on reducing the energy consumption, some specialise on minimizing the delay and different schemes address each. The basic crosstalk model for an on-chip bus is given in Figure-1.

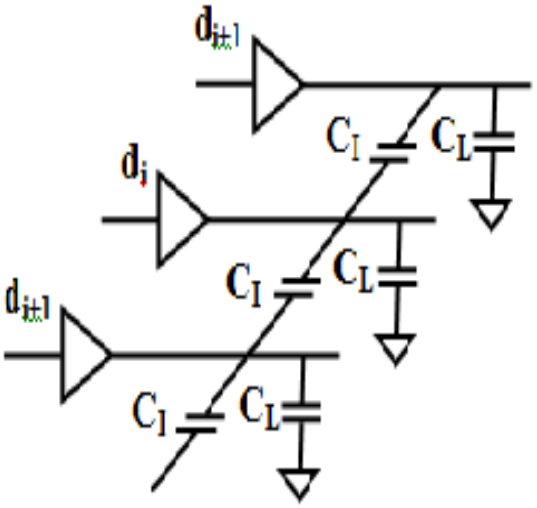

Figure-1. Simplified on-chip bus model with crosstalk.

4. TYPES OF CROSSTALK

Various sorts of crosstalk in a 3-bit bus model is shown in Figure-1 and tabulated in Table-1. Generally crosstalk can be classified into 5 types: Type 0, Type 1, Type 2, Type 3 and Type 4. In Type 0 coupling, the net capacitance is zero because all the lines point the same direction. [13] When there is activity in more than two wires, then, we can say it as Type 1. A Type 2 coupling happens whenever the transition of the centre wire is opposite from the other wires. The case where ever the centres wire undergoes transition with anybody of the other wires. The case wherever the centre wire undergoes transition with anybody of the opposite wires whereas the third one is stable is taken as sort three category of crosstalk, transitions in each adjacent wire will cause sort four category.

Table-1. Types of crosstalk in a 3 bit bus model.

Type 0	Type 1	Type 2	Type 3	Type 4
- - -	- - ↑	- ↑ -	- ↑ ↓	↓ ↑ ↓
↓ ↓ ↓	- ↑ ↑	↑ - ↑	- ↓ ↑	↑ ↓ ↑
↑ ↑ ↑	↑ - -	↑ - ↓	↑ ↓ -	
	↑ ↑ -	↑ ↑ ↓	↓ ↑ -	
	- - ↓	↑ ↓ ↓		
	- ↓ ↓	- ↓ -		
	↓ - -	↓ - ↓		
	↓ ↓ -	↓ - ↑		
		↓ ↓ ↑		
		↓ ↑ ↑		

↑: 0 *to* 1 *transition*
↓: 1 *to* 0 *transition*
– : *no transition*

From the main points we will conclude that sort four appears to be the worst among the five sorts of coupling and desires to be eliminated utterly for dynamic power dissipation to be reduced. From the outline concern crosstalk classification we will say that sort four patterns ends up in most power leakage and delay. Therefore the two patterns of the category 101 and 010 are called impermissible pattern free code.

5. EXISTING TECHNIQUES

Several encoding techniques were proposed like traditional type Fibonacci technique (NFF), Redundant Fibonacci (RF) Coding technique, complement redundant Fibonacci (CRF) codeword.

A. NFF Technique

We describe NFF technique in two parts, namely, data encoding and knowledge transmission. For knowledge encoding, we tend to use normal-form Fibonacci number system of order a pair of. [3] For a -bit dataword d = d_{n-1} $d_{n-2...}d_{0,}$ mistreatment the NFF technique, the distinctive bit codeword nc= cm-1cm-2….c0 are often generated mistreatment NFF encoding algorithmic as shown in Table-2.

Hence, NFF technique will implement (n,b,[n/2])-NAT coding technique, and the other way around. Singularity property of the normal-form Fibonacci number system of order pair of prohibits two consecutive 1's to gift in code words. Table-3, we will see that NFF codewords don't contain adjacent 1s. Table-3 provides 4-bit code words for 3-bit data words.

Table-2. NFF encoding algorithm.

Input: d;
  $r_m = d$;
  for $k = m - 1$ to 1 **do**
    if $r_{k+1} < f_k$ **then**
      $c_k = 0$;
    else
      $c_k = 1$;
    end if
    $r_k = r_{k+1} - f_k \cdot c_k$;
  end for
  $c_0 = r_1$;
Output: $c_{m-1}c_{m-2}\cdots c_0$;

Table-3. 1 bit to 4 bit data code word.

NFF_1	NFF_2	NFF_3	NFF_4
1	2 1	3 2 1	5 3 2 1
0	0 0	0 0 0	0 0 0 0
1	0 1	0 0 1	0 0 0 1
	0 0	0 1 0	0 0 1 0
		1 0 0	0 1 0 0
		1 0 1	0 1 0 1
			1 0 0 0
			1 0 0 1
			1 0 1 0

B. Redundant Fibonacci (RF) coding technique

In the case of NFF technique, Fibonacci numbers are thought about as the basis parts to get bit codewords. Just like the NFF technique, in redundant Fibonacci (RF) coding technique, we tend to contemplate Fibonacci numbers because the basis parts with the exception that's used twice [1]. That is, so as to get bit RF codewords, we tend to contemplate because the basis parts. As is taken into account doubly within the RF technique, we tend to sets of RF codewords every may be a complement of the opposite we tend to contemplate these two sets as redundant Fibonacci [RF] and complement redundant Fibonacci[CRF] codeword sets. Hence, the encoding logic given in [9] is often used for implementing the RF technique. CRF codewords square measure generated by taking bit-wise complement of each codeword from the set of RF codewords. Let be the set of bit CRF codewords [3]. Table-3 shows 1-bit to 4-bit CRF codewords. Table-4 shows CRF encoding algorithm. Third and fourth columns of Table-5 provide 4-bit NFF, RF and CRF codewords, severally, for given 3-bit dataword

Table-4. CRF encoding algorithm.

Input: d;
  $r_m = d$;
  for $k = m - 1$ to 1 **do**
    if $r_{k+1} < f_{2\lceil \frac{k-1}{2} \rceil}$ **then**
      $c_k = 0$;
    else
      $c_k = 1$;
    end if
    $r_k = r_{k+1} - f_{k-1} \cdot c_k$;
  end for
  $c_0 = r_1$;
Output: $c_{m-1}c_{m-2}\cdots c_0$;

Table-5. NFF, RF, CRF codes for 3bit dataword.

DATA WORD	FIBONACCI CODE WORD		
4 2 1	5 3 2 1	3 2 1 1	3 2 1 1
0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
0 0 1	0 0 0 1	0 0 0 1	0 0 1 0
0 1 0	0 0 1 0	0 1 0 0	0 0 1 1
0 1 1	0 1 0 0	0 1 0 1	1 0 0 0
1 0 0	0 1 0 1	0 1 1 1	1 0 1 0
1 0 1	1 0 0 0	1 1 0 0	1 0 1 1
1 1 0	0 0 0 1	1 1 0 1	1 1 1 0
1 1 1	1 0 1 0	1 1 1 1	1 1 1 1

6. PROPOSED ENCODING TECHNIQUE

Figure-2 represents the proposed encoding algorithm for without crosstak data output. During this algorithm data input is regenerate into Fibonacci codes.after that we have to envision intial 3bits if crosstalk is present means we have to do bitswapping method. Is same as last 3bits also. If data input doesn't having crosstalk so data input is taken as output. If first 3 bits having crosstalk means apply bit swapping method and there is no crosstalk in last 3bit means add the remaining bit and vice versa. The below examples are represent the above concept. Figure-2 represents the proposed algorithm. Here xxxx is nothing but any 4bit data like 1010, 1101etc.

A. Proposed encoding algorithm

Step-1: Get the 4bit data input in the form of Fibonacci

Step-2: From the given input initially check first 3bits of the input.

Step-3: If the first 3bits of the input is 101 or 010.then bits swapping takes place in which the ultimate output will be either in the form of 011 or 001.

Step-4: If the 3bits of the input is not 101 or 010 then go the last 3bits of the given input.

Step-5: Similarly the last 3bits of the input is 101 or 010.then bits swapping takes place in which the ultimate output will be either in the form of 011 or 001.

Step-6: If the last 3bits of the input is not 101 or 010 then go to the given data input.

Eg1

100 ⟶ 010 ⟶ 1001

Eg2

001 ⟶ 0001 ⟶ 0001

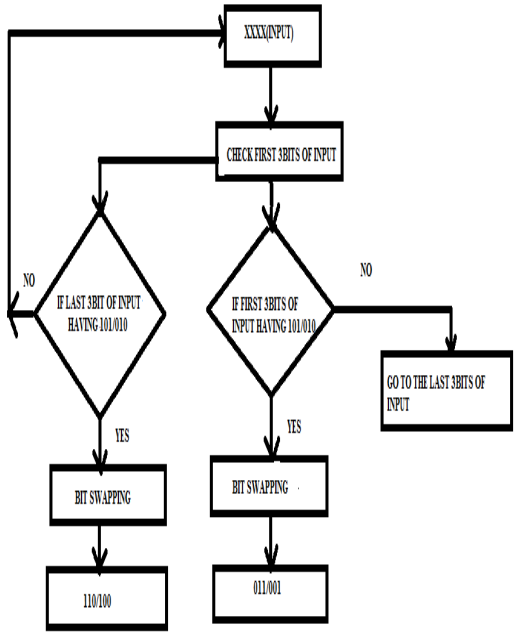

Figure-2. Proposed encoding algorithm.

Figure-2, proposed encoding algorithm for without crosstalk. Here the proposed algorithm is minimize the crosstalk and eliminate the forbidden patterns 010, 101 totaly. This algorithm is simulated by MODELSIM software also power and area is calculated.

B. Proposed table

Table-6 represents the without crosstalk for 3input data.

Table-6. Proposed encoding algorithm table.

Data input	Fibonacci codes	Proposed output
000	0000	0000
001	0001	0001
010	0**010**	0001
011	**010**0	1000
100	0**101**	1001
101	1000	1000
110	1001	1001
111	**1010**	0110

7. SIMULATION RESULTS

The final results are simulated with MODEL SIM software. And its power is calculated using quartus-11software

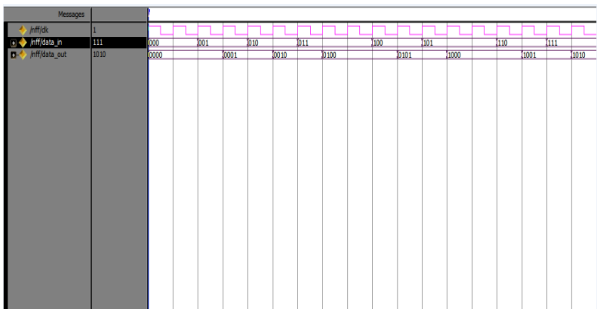

Figure-3. NFF simulation output for existing.

Figure-3 shows the NFF simulation output. In this clk, data-in are inputs and data-out is represented as output. Consider the values given for data-in=111 and the output is1010.

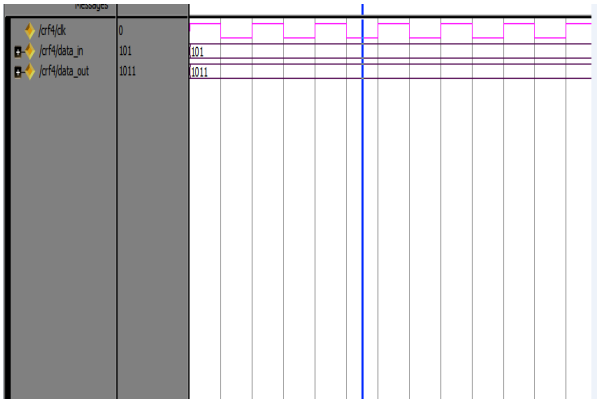

Figure-4. CRF simulation output for existing.

Figure-4 shows the CRF simulation output. In this clk, data-in are inputs and data-out is represented as output. Consider the values given for data-in=101 and the output is1011.

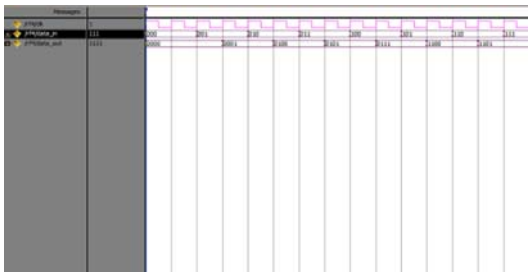

Figure-5. RF simulation output for existing.

Figure-5 shows the RF simulation output. In this clk, data-in are inputs and data-out is represented as output. Consider the values given for data-in=111 and the output is1111.

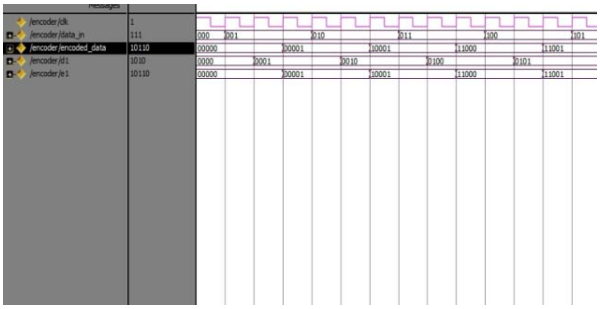

Figure-6. Proposed algorithm simulation output for encoding.

Figure-6 shows the encoding algorithm1 simulation output. In this clk, data-in are inputs and e1 is represented as output. Consider the values given for data-in=111 and the output is 10110.

8. RESULTS AND DISCUSSIONS

Power and area calculated using quartus-11 software.

Table-7.

Parameter	Existing technique	Proposed technique
Power	323mw	64.71mw
No. of slices	4	2
No. of flip flops	8	3
No. of bonded Iob	8	4
Fanout	2.47	2.27

9. CONCLUSIONS

In this paper, an efficient algorithm is designed using the concept of Fibonacci numbers. Also 3bit data is directly converted into without crosstalk data. Crosstalk avoidance codes are shown to be able to reduce the inter-wire crosstalk and therefore boost the maximum speed on the data bus. The capacitance model gives line-to-line and line-to-ground capacitances separately, and lead to precise delay and crosstalk estimations the worst-case inductance occurs when adjacent lines transition in the same direction. The proposed algorithms are minimizing the crosstalk and eliminate the 010 and 101 patterns totally. The output parameter is analysed and compared by using Xilinx software. The output is simulated by MODELSIM 6.4. power, number of slices, number of flip-flops number of bonded IOB's switching capacity of the interconnects, glitches, area are reduced. This algorithm can be adopted for data communication and security purposes.

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